JTAGPPC Controller (v2.01c)

DS298 April 24, 2009 **Product Specification**

Introduction

The JTAGPPC Controller is a wrapper for the JTAGPPC and JTAGPPC440 FPGA primitives. The JTAGPPC and JTAGPPC440 primitives allow the PowerPC® 405 processor and the PowerPC 440 processor, respectively, to connect to the JTAG chain of the FPGA. For more information about connecting the PPC405 processor to the FPGA JTAG chain, refer to the JTAG Debug Port section of the *PowerPC 405 Processor Block Reference Guide*. For more information about connecting the PowerPC 440 processor to the FPGA JTAG chain, refer to the JTAG Interface section of UG200, *Embedded Processor Block in Virtex®-5 FPGAs Reference Guide*.

Features

- Wrapper for the JTAGPPC and JTAGPC440 primitives
- Enables the debug port of the PowerPC to be connected to the FPGA JTAG chain
- Can connect up to two PowerPC primitives
- Automatically instantiates and connects second unused PowerPC processor in any dual-PowerPC device

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	See EDK Supported Device Families.	
Version of Core	jtagppc_cntlr	v2.01c
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	0	1
FFs	0	0
Block RAMs	0	0
Special Features	In Virtex-4: JTAGPPC In Virtex-5: JTAGPPC440	
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Reference Designs	None	
Design Tool Requirements		
Xilinx Implementation Tools	See Tools for requirements.	
Verification		
Simulation		
Synthesis		
Support		
Provided by Xilinx, Inc.		

Functional Description

The JTAGPPC Controller shown in Figure 1 is a wrapper for the JTAGPPC and JTAGPPC440 FPGA primitives.

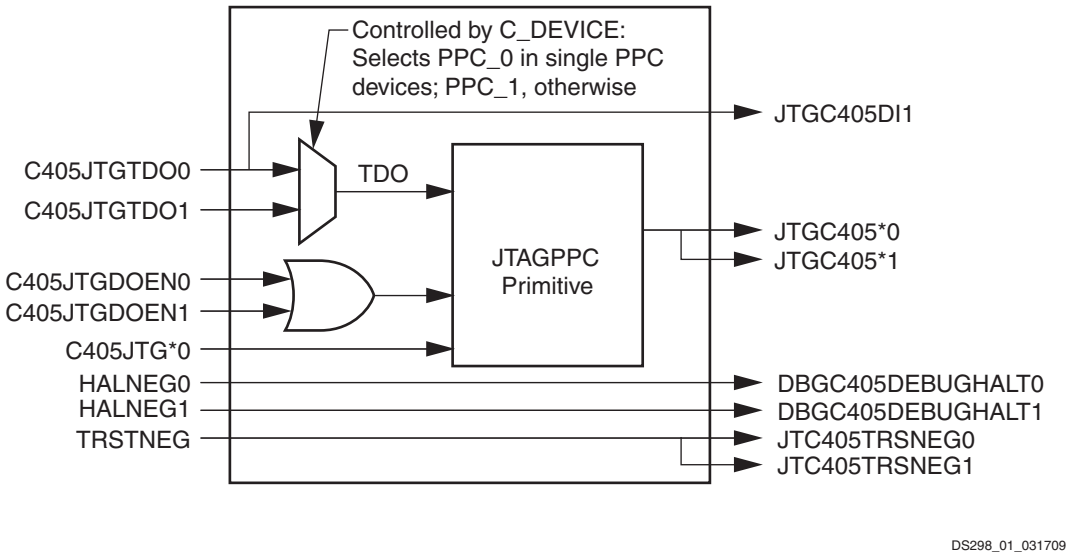

Figure 1: **JTAGPPC Controller Block Diagram**

In FPGA devices containing two PowerPC processor blocks (as listed in Table 2), if the JTAGPPC Controller is used to connect any PowerPC to the FPGA JTAG chain, then the design netlist must instantiate both PowerPC processors and connect both of them to the JTAGPPC Controller, even if the second PowerPC processor instance is unused in the application. Beginning with Version 2.01, the JTAGPPC Controller wrapper automatically instantiates and connects the second unused PowerPC processor if it is not already instantiated in the design.

JTAGPPC Controller I/O Signals

The I/O signals for the JTAGPPC Controller are listed and described in Table 1. All signals listed in Table 1 are compatible with both the PowerPC 405 and PowerPC 440 processors.

Table 1: **JTAGPPC Controller I/O Signals**

Signal Name	Interface	I/O	Initial State	Description
TRSTNEG[1]	SYSTEM	I		JTAG Reset signal from user/external logic for all PowerPC processors
HALTNEG0[1]	SYSTEM	I		Processor Halt signal to first PowerPC
DBGC405DEBUGHALT0[1]	PPC_0	O	HALTNEG0	Halt signal to first PowerPC
C405JTGTDO0[(1)]	PPC_0	I		JTAG TDO signal from first PowerPC
C405JTGTDOEN0[1]	PPC_0	I		JTAG TDOEN signal from first PowerPC
JTGC405TRSTNEG0[1]	PPC_0	O	TRSTNEG	JTAG Reset signal to first PowerPC
JTGC405TCK0[1]	PPC_0	O	same as primitive	JTAG TCK signal to first PowerPC

Table 1: **JTAGPPC Controller I/O Signals *(Cont'd)***

Signal Name	Interface	I/O	Initial State	Description
JTGC405TDI0[1]	PPC_0	O	same as primitive	JTAG TDI signal to first PowerPC
JTGC405TMS0[1]	PPC_0	O	same as primitive	JTAG TMS signal to first PowerPC
HALTNEG1[2]	SYSTEM	I		Processor Halt signal from user/external logic (Ex: Vision Probe)
DBGC405DEBUGHALT1[2]	PPC_1	O	HALTNEG1	Halt signal to second PowerPC
C405JTGTDO1[(2)]	PPC_1	I		JTAG TDO signal from second PowerPC
C405JTGTDOEN1[(2)]	PPC_1	I		JTAG TDOEN signal from second PowerPC
JTGC405TRSTNEG1[(2)]	PPC_1	O	TRSTNEG	JTAG Reset signal to second PowerPC
JTGC405TCK1[(2)]	PPC_1	O	same as primitive	JTAG TCK signal to second PowerPC
JTGC405TDI1[(2)]	PPC_1	O	same as primitive	JTAG TDI signal to second PowerPC
JTGC405TMS1[(2)]	PPC_1	O	same as primitive	JTAG TMS signal to second PowerPC

1. Must be connected if core is used.
2. Should be left unconnected in designs that do not contain a second PowerPC instance.

JTAGPPC Controller Parameters

The parameters for the JTAGPPC Controller are listed in Table 2.

Table 2: **JTAGPPC Controller Parameters**

Parameter Name	Description	Allowed Values	Tool Calculated	Type
C_DEVICE	Target device identifier. Used to determine how many PowerPC primitives exist in the part.	Single PowerPC devices: 4VFX12, 4VFX20, 5VFX30T, 5VFX70T. Dual PowerPC devices: 4VFX40, 4VFX60, 4VFX100, 4VFX140, 5VFX100T, 5VFX115T, 5VFX130T, 5VFX180T.	yes	string

Allowable Parameter Combinations

There are no restrictions on parameter combinations.

Parameter - Port Dependencies

When C_DEVICE indicates a single PowerPC device (as listed in Table 2), ports DBGC405DEBUGHALT1, C405JTGTDO1, C405JTGTDOEN1, JTGC405TRSTNEG1, JTGC405TCK1, JTGC405TDI1 and JTGC405TMS1 must remain unconnected.

When C_DEVICE indicates a dual PowerPC device (as listed in Table 2), ports DBGC405DEBUGHALT1, C405JTGTDO1, C405JTGTDOEN1, JTGC405TRSTNEG1, JTGC405TCK1, JTGC405TDI1 and JTGC405TMS1 must be connected to the second PowerPC instance only if it is instantiated in the design.

JTAGPPC Controller Register Descriptions

Not applicable.

JTAGPPC Controller Interrupt Descriptions

Not applicable.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Reference Documents

- *PowerPC 405 Processor Block Reference Guide*
- UG200, *Embedded Processor Block in Virtex-5 FPGAs Reference Guide*

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
8/12/2008	1.0	Initial Release.
4/24/2009	2.0	Removed support for Virtex-II devices. Replaced references to supported device families and tool names with hyperlink to PDF file.

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