Instruction Side OCM Bus v1.0 (v2.00b)

DS479 April 24, 2009 **Product Specification**

Introduction

The ISOCM_V10 is an instruction-side On-Chip Memory (OCM) bus interconnect core. The core connects the PowerPC® 405 processor instruction-side OCM interface to one or more peripherals, typically to the instruction-side OCM BRAM controller (ISBRAM_IF_CNTRL). For information about the PowerPC 405 processor OCM controller interface, see the *PowerPC 405 Processor Block Reference Guide*.

Features

- Single master - no bus arbitration logic
- Configurable multiple slave capability - contains read-data multiplexing when used with 2 or more slaves

LogiCORE® IP Facts	
Core Specifics	
Supported Device Family	See EDK Supported Device List.
Resources Used	See Table 4.
Special Features	Add if applicable
Provided with Core	
Documentation	Product Specification
Design File Formats	VHDL
Constraints File	N/A
Verification	N/A
Instantiation Template	N/A
Additional Items	N/A
Design Tool Requirements	
Xilinx Implementation Tools	See Tools for requirements.
Verification	
Simulation	
Synthesis	
Support	
Provided by Xilinx, Inc.	

Functional Description

The ISOCM_V10 is an instruction-side On-Chip Memory (OCM) bus interconnect core which connects the PowerPC 405 processor instruction-side OCM interface to one or more peripherals. The block diagram for the core is shown in Figure 1, while the core signals are listed and described in Table 1.

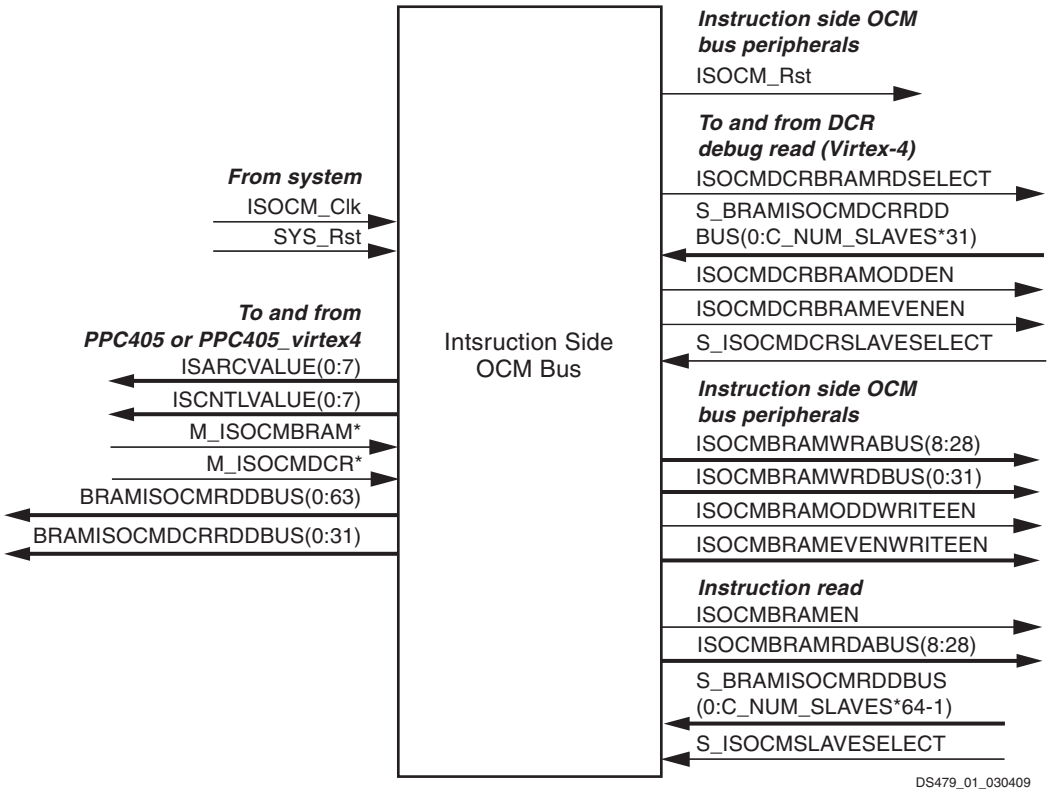

Figure 1: **Instruction Side OCM Bus Block Diagram**

Instruction Side OCM Bus I/O Signals

The ISOCM Bus signals are listed and described in Table 1.

Table 1: **Instruction Side OCM Bus I/O Signals**

Signal	I/O	Connects to	Description
ISBRAMCLK	I	system	Unused
SYS_Rst	I	system	Drives the output ISOCM_RST
ISOCM_RST	O	isbram_if_cntlr	Reset signal for ISOCM BRAM interface controllers (isbram_if_cntlr)
M_ISOCMBRAM RDABUS	I	ppc405	Drives the output ISOCMBRAMRDABUS
M_ISOCMBRAM WRABUS	I	ppc405	DCR access address (ISINIT). Drives the output ISOCMBRAMWRABUS
M_ISOCMBRAMEN	I	ppc405	Drives the output ISOCMBRAMEN

Table 1: **Instruction Side OCM Bus I/O Signals** ***(Cont'd)***

Signal	I/O	Connects to	Description
M_ISOCMBRAM WRDBUS	I	ppc405	Drives the output ISOCMBRAMWRDBUS
M_ISOCMBRAM ODDWRITEEN	I	ppc405	Drives the output ISOCMBRAMODDWRITEEN
M_ISOCMBRAM EVENWRITEEN	I	ppc405	Drives the output ISOCMBRAMEVENWRITEEN
M_ISOCMDCR BRAMODDEN	I	ppc405	Drives the output ISOCMDCRBRAMODDEN (Virtex®-4 only)
M_ISOCMDCR BRAMEVENEN	I	ppc405	Drives the output ISOCMDCRBRAMEVENEN (Virtex-4 only)
M_ISOCMDCR BRAMRDSELECT	I	ppc405	Drives the output ISOCMDCRBRAMRDSELECT (Virtex-4 only)
S_BRAMISOCM RDDBUS	I	isbram_if_cntlr	Drives the output BRAMISOCMRDDBUS
S_BRAMISOCM DCRRDDBUS	I	isbram_if_cntlr	Drives the output BRAMISOCMDCRRDDBUS (Virtex-4 only)
S_ISOCMSLAVE SELECT	I	isbram_if_cntlr	Acknowledge signal from addressed slave. Used as a read-data valid for S_BRAMISOCMRDDBUS in multi-slave system
S_BRAMISOCMDCR SLAVESELECT	I	isbram_if_cntlr	Acknowledge signal from addressed slave. Used as a read-data valid for S_BRAMISOCMDCRRDDBUS in multi-slave system (Virtex-4 only)
BRAMISOCM RDDBUS	O	ppc405	Instruction read data
ISARCVALUE	O	ppc405	ISOCM 16MB address window offset. The signal value is defined by C_ISARCVALUE
ISCNTLVALUE	O	ppc405	ISOCM setup. The signal value is defined by the parameter C_ISCNTLVALUE
ISOCMBRAMEN	O	isbram_if_cntlr	Instruction BRAM enable
ISOCMBRAM WRDBUS	O	isbram_if_cntlr	DCR write data using ISFILL
ISOCMBRAMODD WRITEEN	O	isbram_if_cntlr	DCR write enable using ISINIT(29)
ISOCMBRAMEVEN WRITEEN	O	isbram_if_cntlr	DCR write enable using ISINIT(29)
ISOCMBRAM RDABUS	O	isbram_if_cntlr	Instruction fetch address
ISOCMBRAM WRABUS	O	isbram_if_cntlr	DCR write address using ISINIT(8:28)
ISOCMDCRBRAM ODDEN	O	isbram_if_cntlr	DCR enable using ISINIT(29) (Virtex-4 only)

Table 1: **Instruction Side OCM Bus I/O Signals *(Cont'd)***

Signal	I/O	Connects to	Description
ISOCMDCRBRAM EVENEN	O	isbram_if_cntlr	DCR enable using ISINIT(29) (Virtex-4 only)
ISOCMDCRBRAM RDSELECT	O	isbram_if_cntlr	DCR enable using ISINIT(29) (Virtex-4 only)
BRAMISOCMDCR RDDBUS	O	ppc405	DCR read data for ISFILL (Virtex-4 only)

For information about the OCM controller interface feature, see the *PowerPC 405 Processor Block Reference Guide*.

Instruction Side OCM Bus Parameters

The ISOCM Bus parameters are listed and described in Table 2.

Table 2: **Instruction Side OCM Bus Parameters**

Parameter	Description	Default	Tool Calculated	Type
C_NUM_ MASTERS	Number of ISOCM masters. The only allowed value is 1	1	Yes	integer
C_NUM_ SLAVES	Number of ISOCM slaves	1	Yes	integer
C_ISARC VALUE	Power-on address offset for the 16 MB ISOCM address window relative to PLB address range. E.g. with C_ISARCVALUE=0x54, the ISOCM memory window will reside in the address range: 0x5400_0000-0x54FF_FFFF.	0x30	Yes	std_logic_ vector
C_ISCNTL VALUE	Power-on configuration of the PowerPC processor ISOCM interface controller. For details, see the "*PowerPC 405 Processor Block Reference Guide*".	0x81	Yes	std_logic_ vector

Allowable Parameter Combinations

There are no restrictions on allowed parameter combinations in this core.

Parameter - Port Dependencies

The ISOCM bus parameter-port dependencies are listed and described in Table 3.

Table 3: **Port and parameter dependencies**

Name	Affects	Depends	Relationship Description
Design Parameters			
C_NUM_SLAVES	S_BRAMISOCMRDDBUS	0 to C_NUM_SLAVES*64-1	Scale width of OCM read data bus based on number of connected slaves
C_NUM_SLAVES	S_BRAMISOCMDCRRDDBUS	0 to C_NUM_SLAVES*32-1	Scale width of DCR read data bus based on number of connected slaves
C_NUM_SLAVES	S_ISOCMSLAVESELECT	0 to C_NUM_SLAVES	Scale width of OCM slave select based on number of connected slaves
C_NUM_SLAVES	S_BRAMISOCMDCRSLAVESELECT	0 to C_NUM_SLAVES	Scale width of DCR slave select based on number of connected slaves
Port Signals			
S_BRAMISOCMRDDBUS		C_NUM_SLAVES	Scale width of OCM read data bus based on number of connected slaves
S_BRAMISOCMDCRRDDBUS		C_NUM_SLAVES	Scale width of DCR read data bus based on number of connected slaves
S_ISOCMSLAVESELECT		C_NUM_SLAVES	Scale width of OCM slave select based on number of connected slaves
S_BRAMISOCMDCRSLAVESELECT		C_NUM_SLAVES	Scale width of DCR slave select based on number of connected slaves

Multi-Slave Configuration

This version of the bus can handle multiple slaves. Slave address ranges must be non-overlapping and each slave core is responsible for its own address range check. All readable slaves must follow one of two methods for returning data:

1. Provide an acknowledge signal (S_ISOCMSLAVESELECT and S_ISOCMDCRSLAVESELECT) which they raise when addressed. When not addressed these signals must be held low. The slave read-data is ignored when the acknowledge is low. The ISOCM bus use the acknowledge signal as a valid signal to multiplex read-data.
2. Always provide a high acknowledge signal, but drive all 0's on read-data when not addressed.

Instruction Side OCM Bus Register Descriptions

There are no registers in this core.

Instruction Side OCM Bus Interrupt Descriptions

There are no interrupts associated with this core.

Design Implementation

Design Tools

The Instruction Side OCM Bus design is handwritten.

Xilinx XST is the synthesis tool used for synthesizing the Instruction Side OCM Bus.

Target Technology

The target technology is an FPGA listed in EDK Supported Device Families.

Device Utilization and Performance Benchmarks

Table 4: **ISOCM_V10 Bus Resource Utilization**

Parameters	DCR read back (Virtex-4 only)	Resources	
		Flip-Flops	4-input LUTs
C_NUM_SLAVES = 1	-	0	0
C_NUM_SLAVES = 2	No	0	64
	Yes	0	96
C_NUM_SLAVES = 3	No	0	128
	Yes	0	196

There are no performance benchmarks available.

Specification Exceptions

Not applicable.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Reference Documents

1. UG018 PowerPC 405 Processor Block Reference Guide
2. DS446 Instruction Side OCM BRAM Interface Controller Data Sheet

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
6/16/04	1.0	Initial Xilinx release
8/17/04	1.1	Updated for EDK 6.3. Updated trademarks and supported device family listing.
9/22/04	1.2	Converted to new data sheet format
8/9/05	1.3	Converted to new DS template; updated Figure 1; reformatted tables.
1/23/07	1.4	Fixed RdDBus mux error for 5 slave case.
4/24/09	1.5	Replaced references to supported device families and tool name(s) with hyperlink to PDF file.

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