


WARP FPGA BOARD

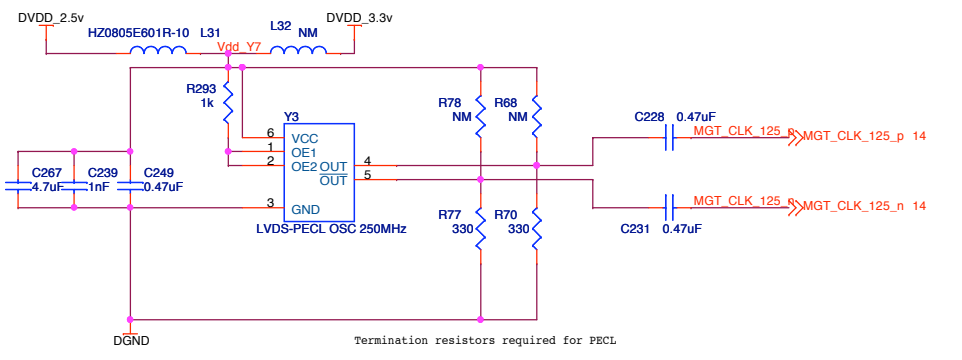
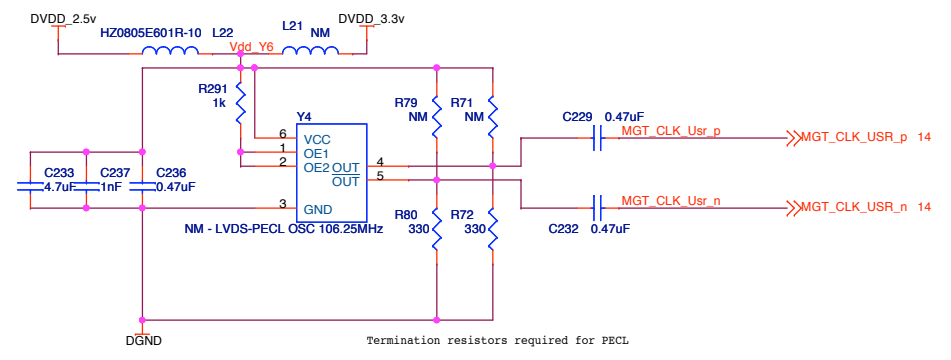
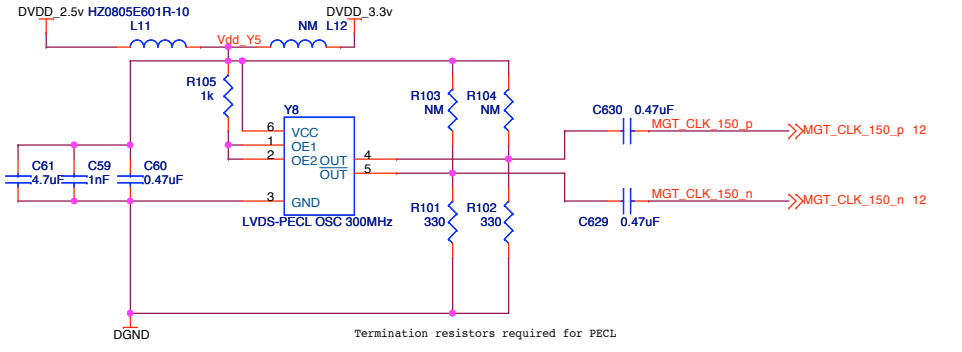
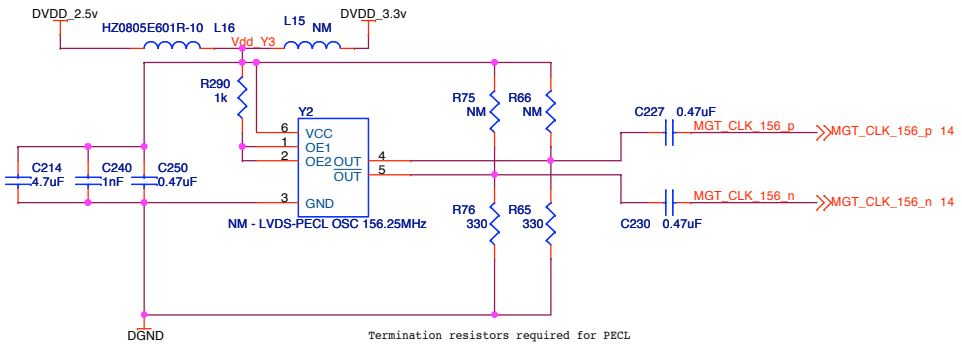
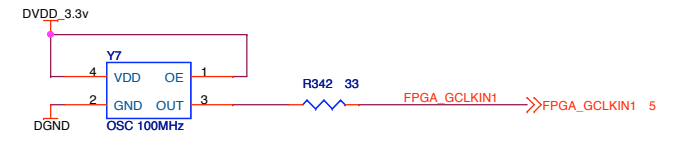
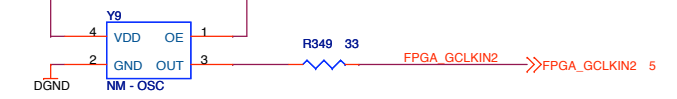
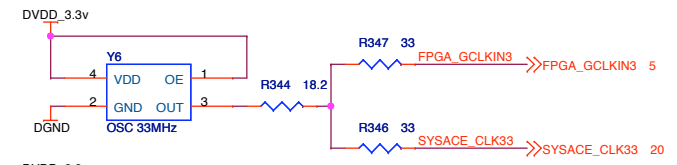
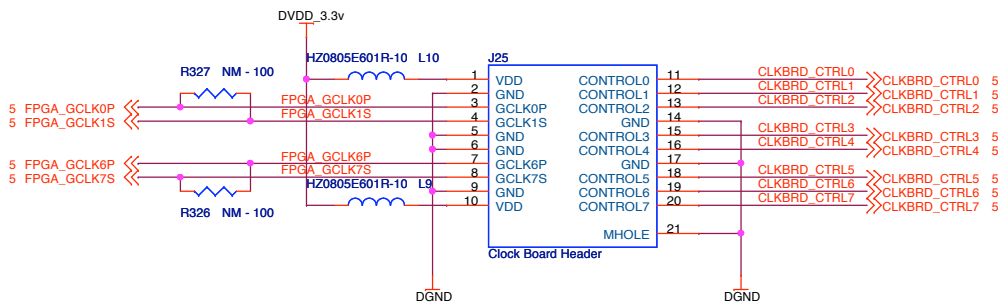
Version 2.2

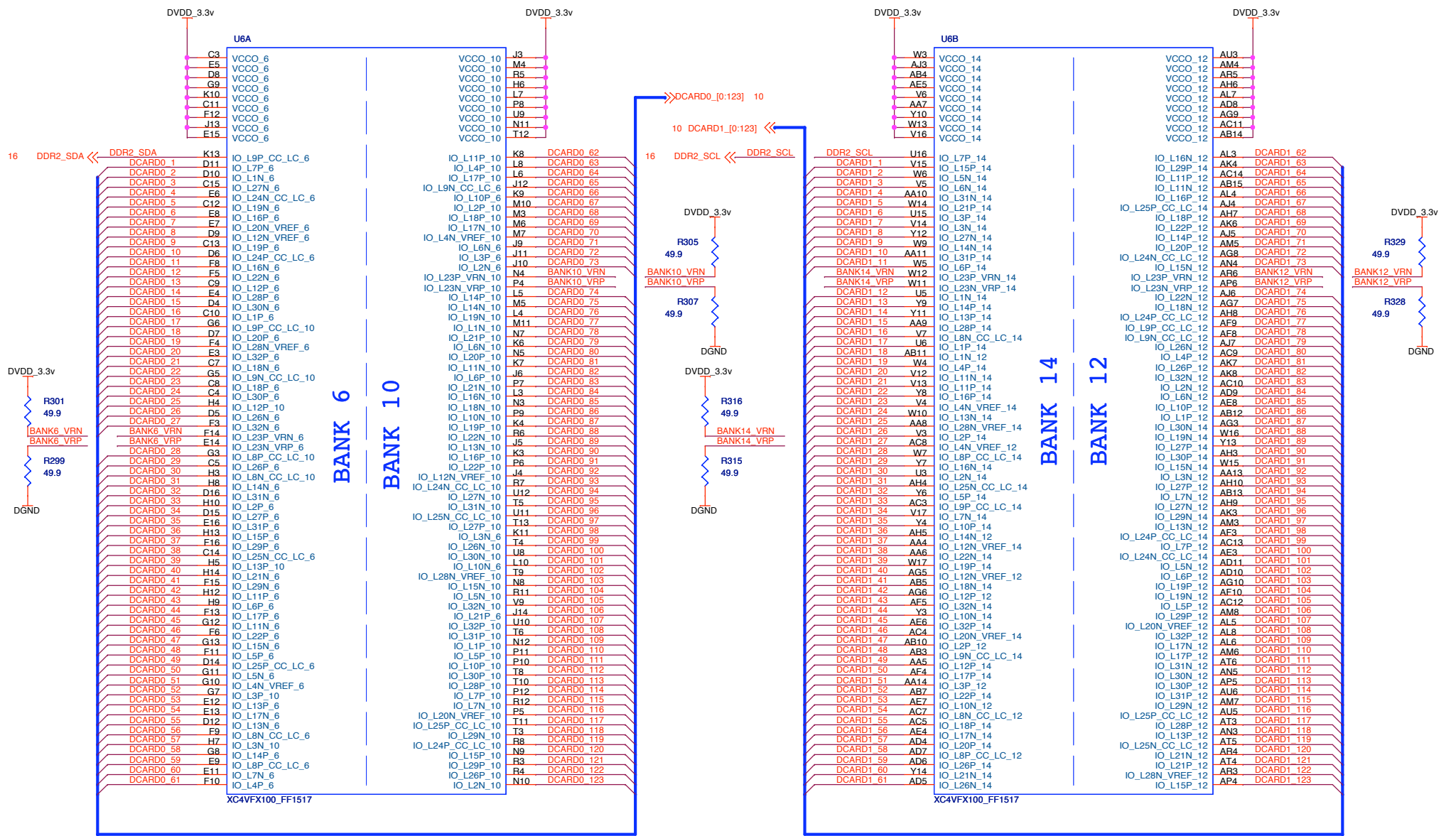
Siddharth Gupta

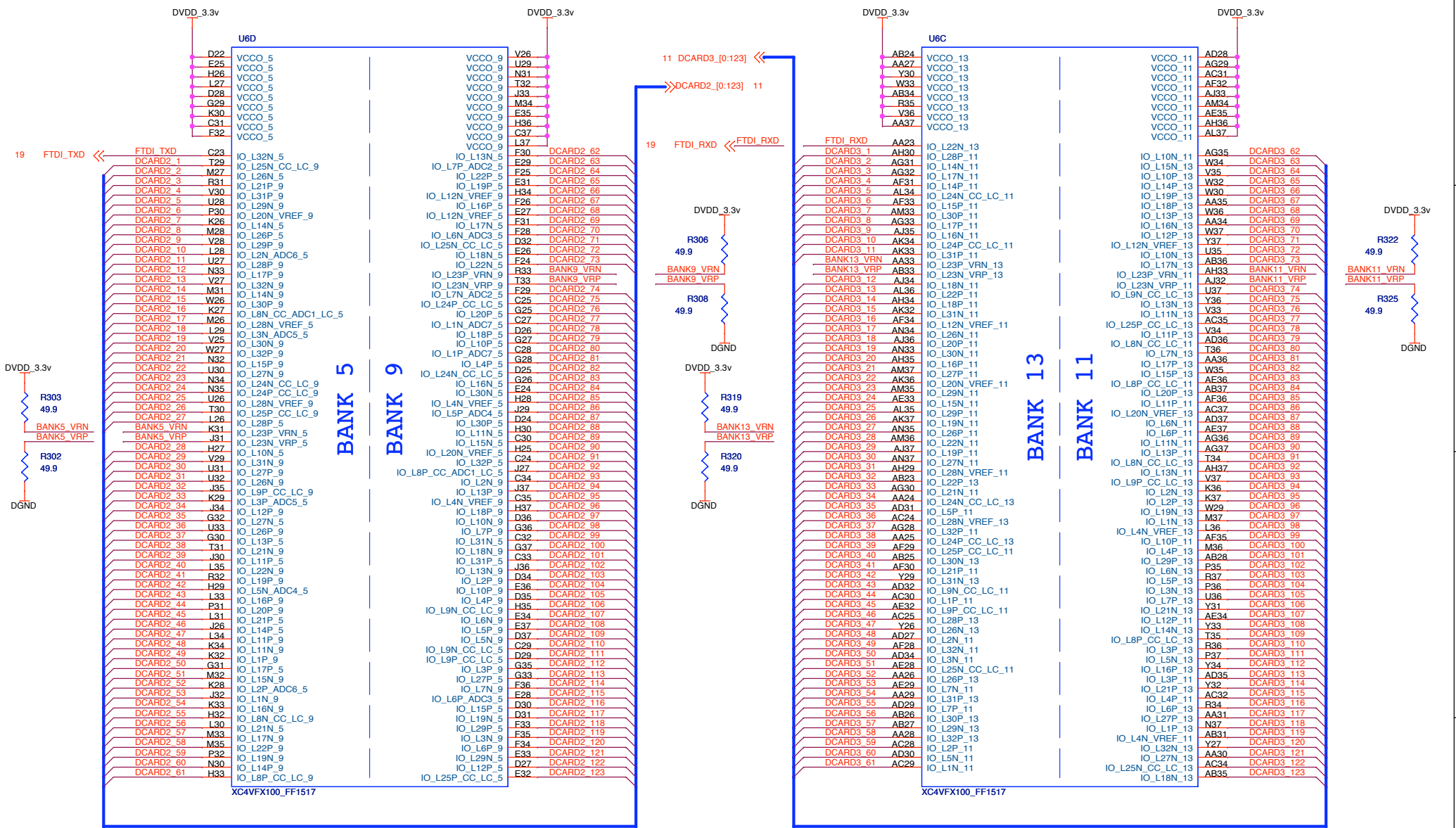
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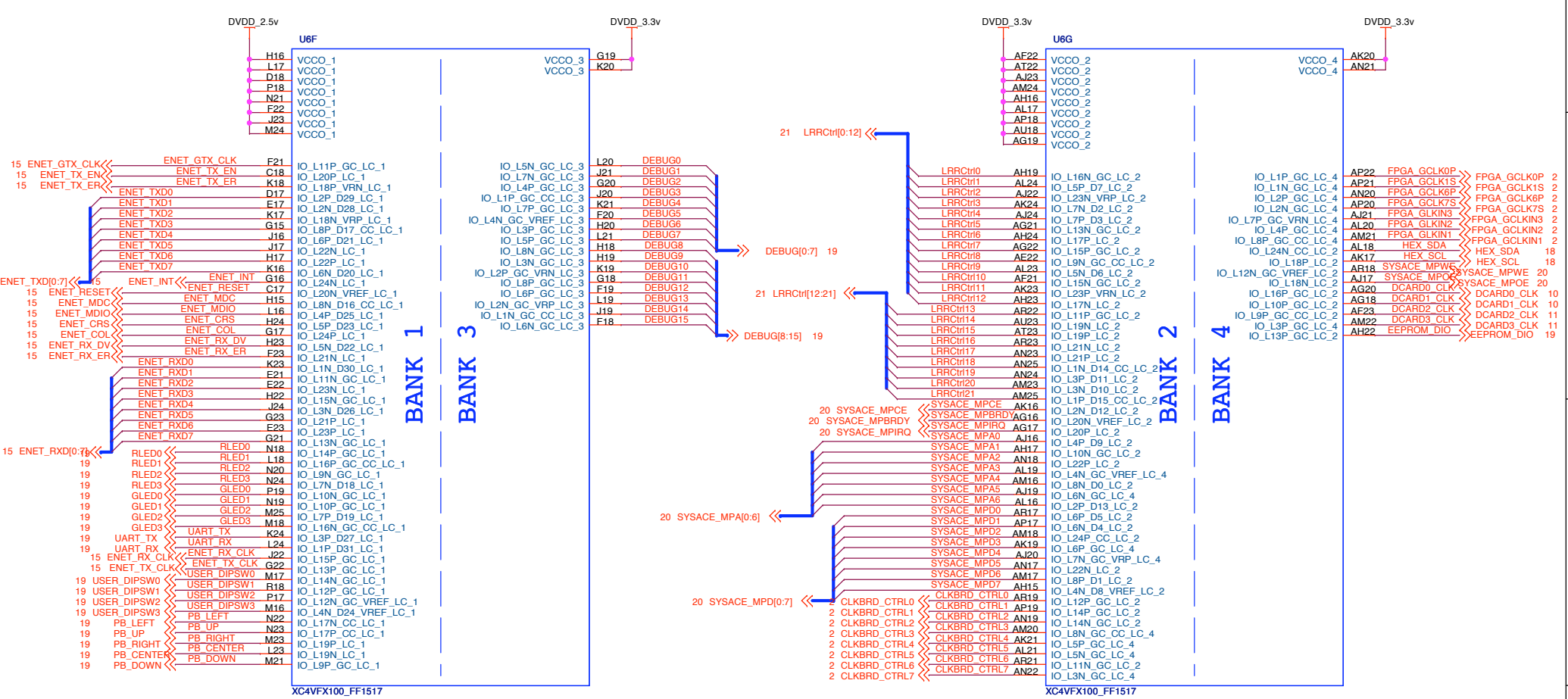
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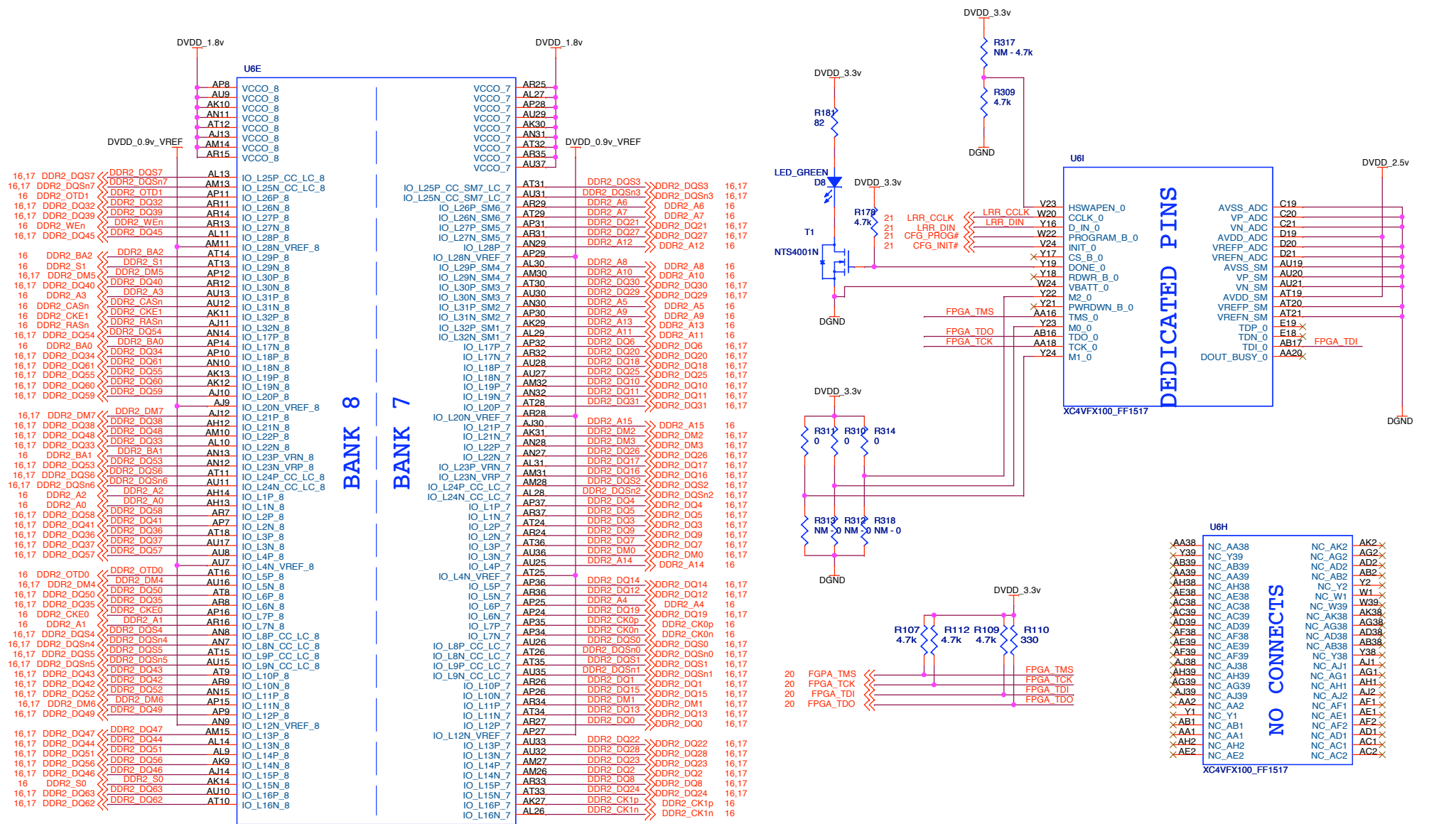


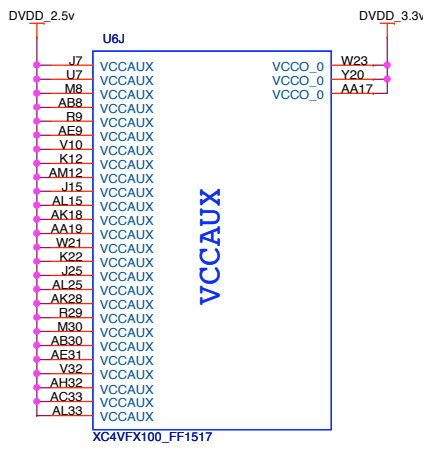
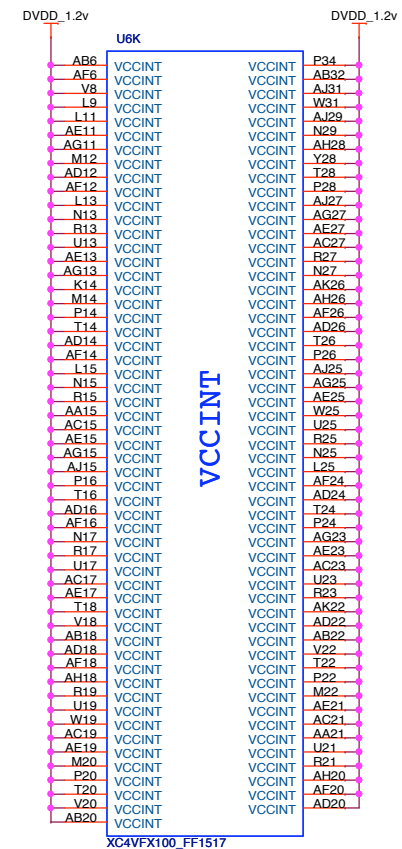
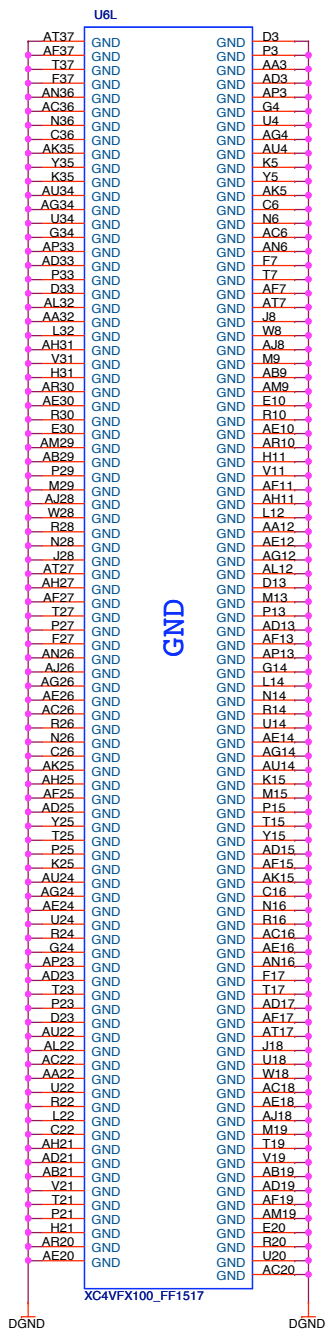




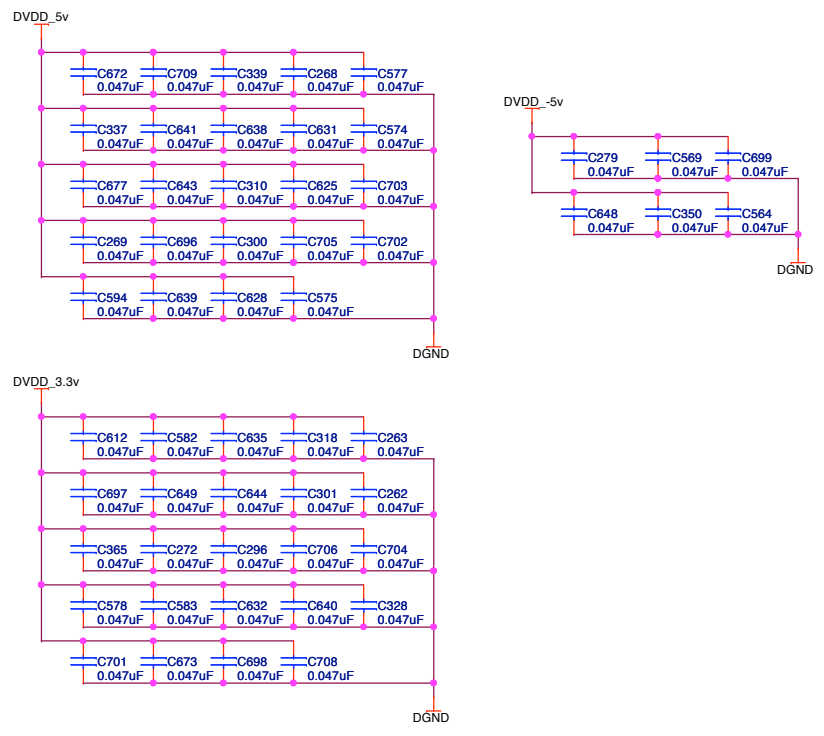
XC4VFX100_FF1517

XC4VFX100_FF1517

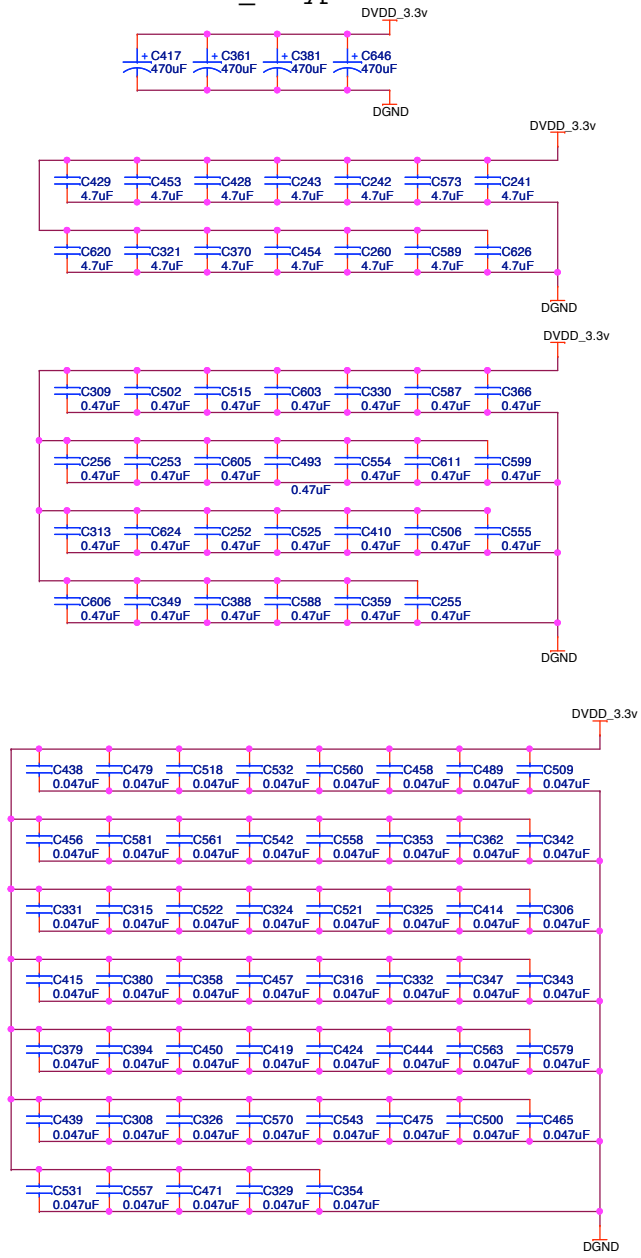




High-speed bypass for Daughtercard Headers



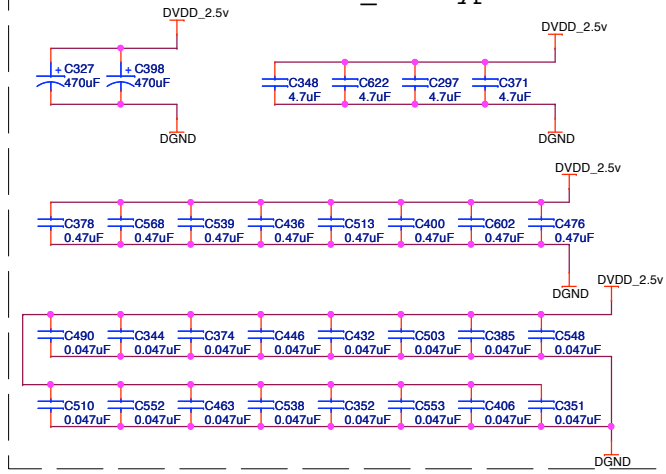
FPGA VCCO_x Bypass 3.3v



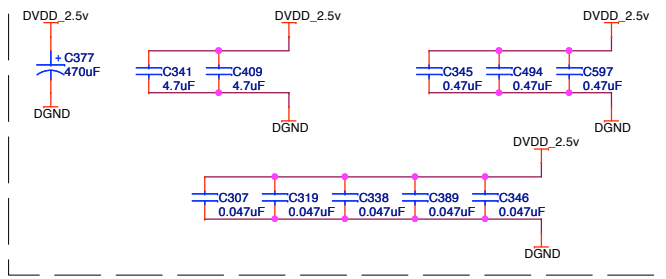
FPGA VCC_INT Bypass



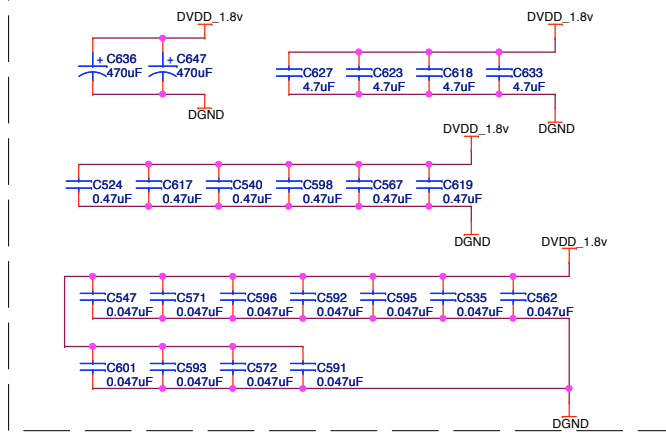
FPGA VCC_AUX Bypass



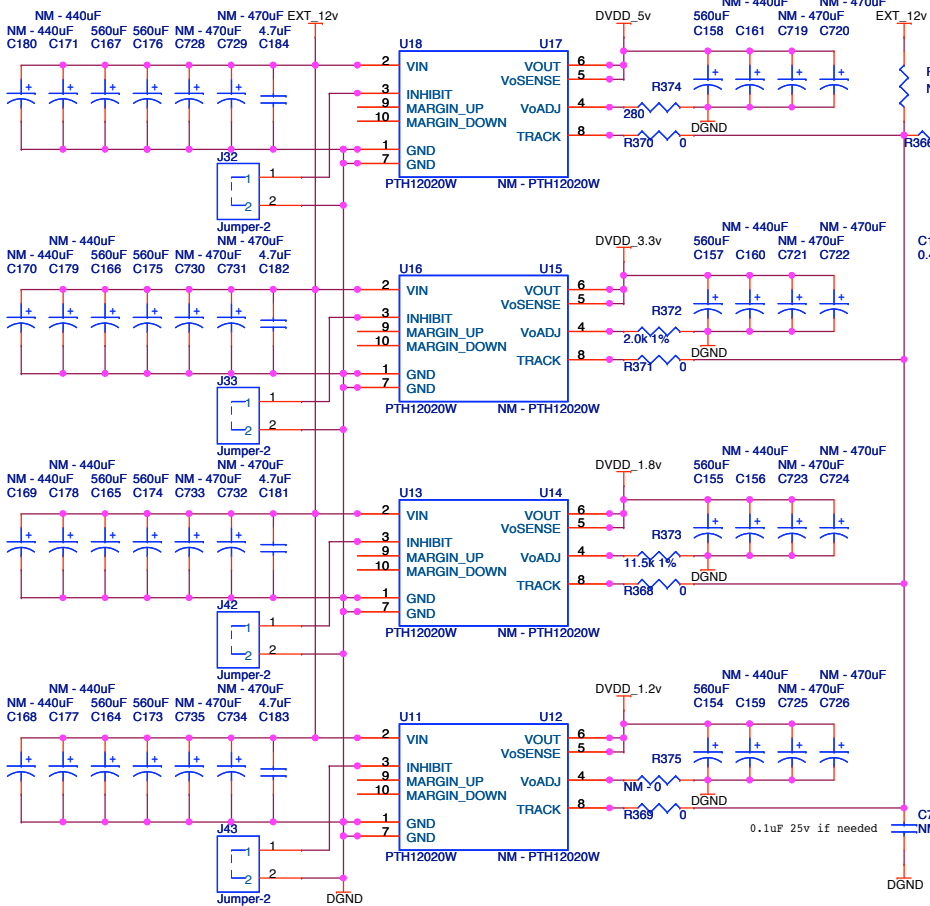
FPGA VCCO_x Bypass 2.5v



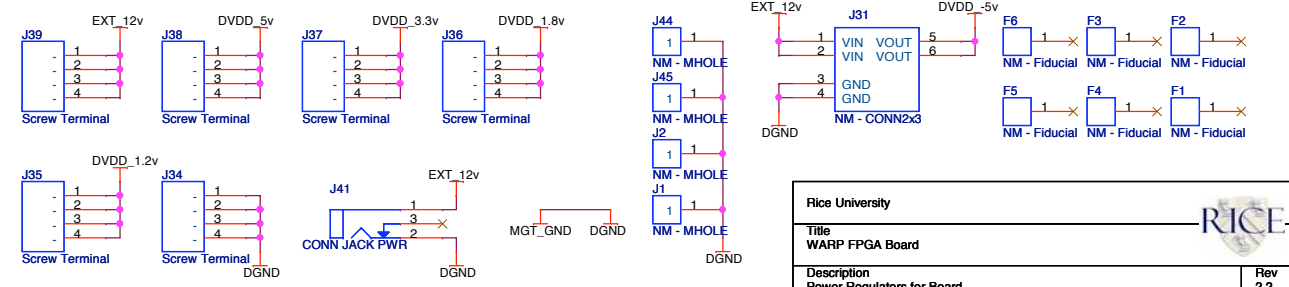
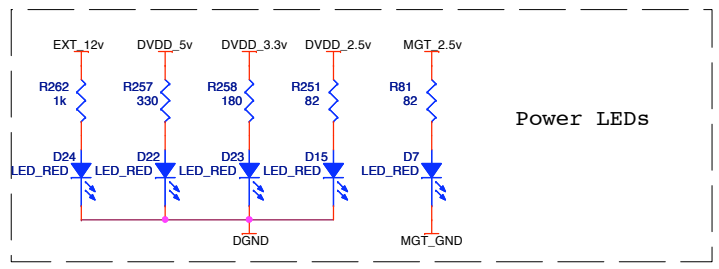
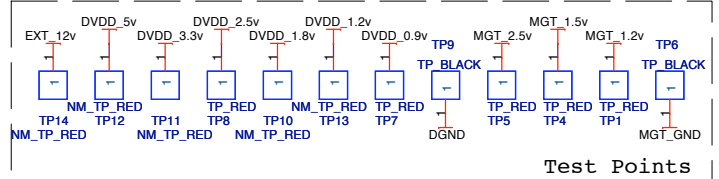
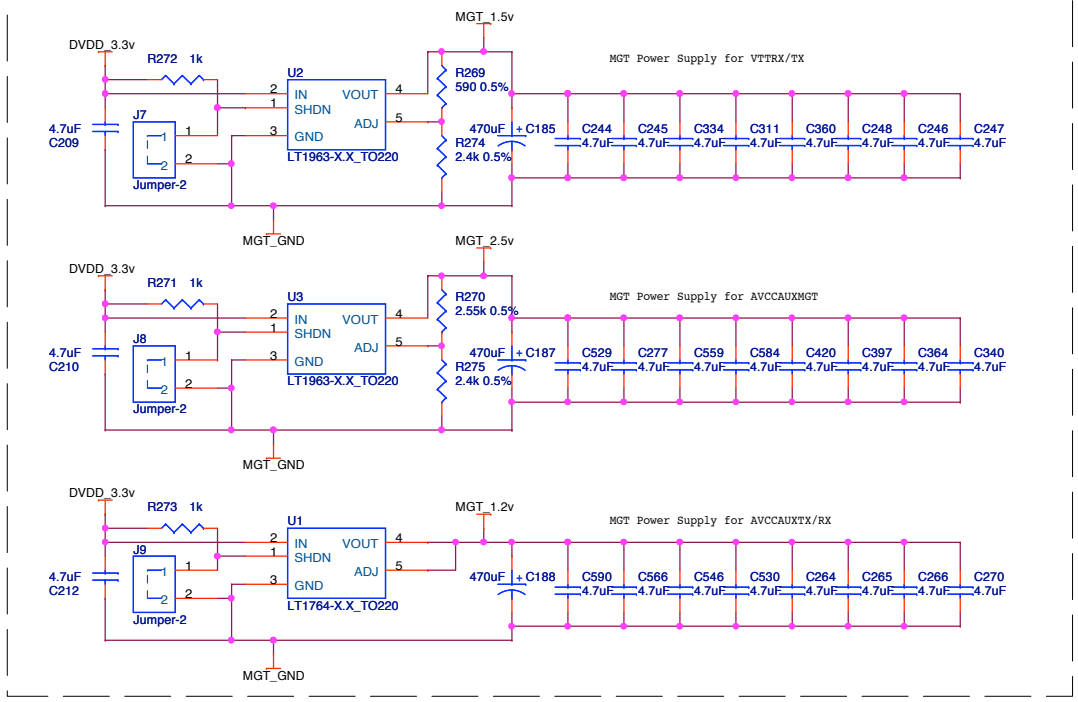
FPGA VCCO_x Bypass 1.8v



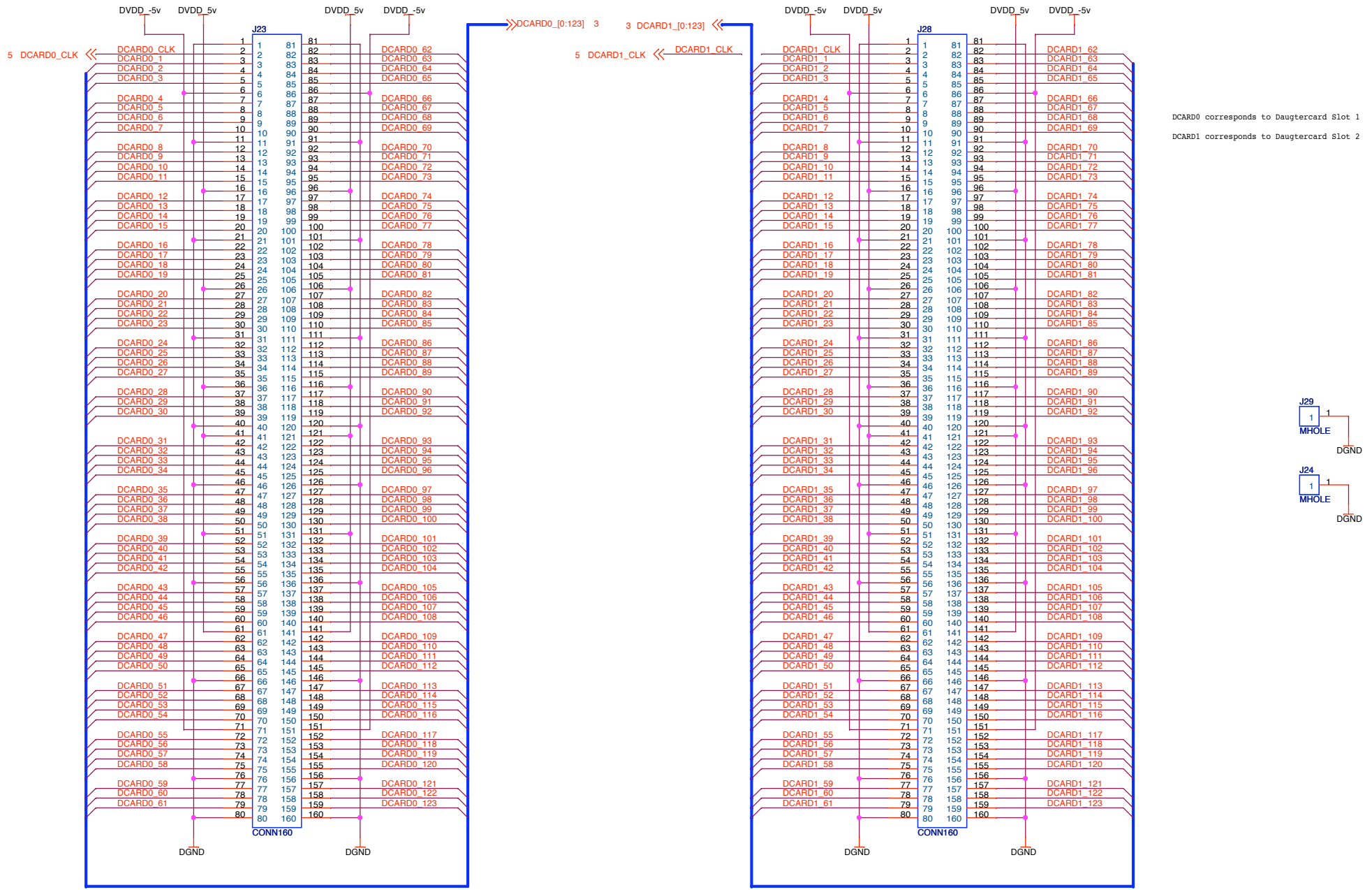
Overlapping duplicate regulators with one set TH and one set SMT



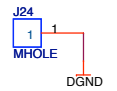
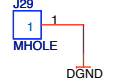
MGT Power Regulators

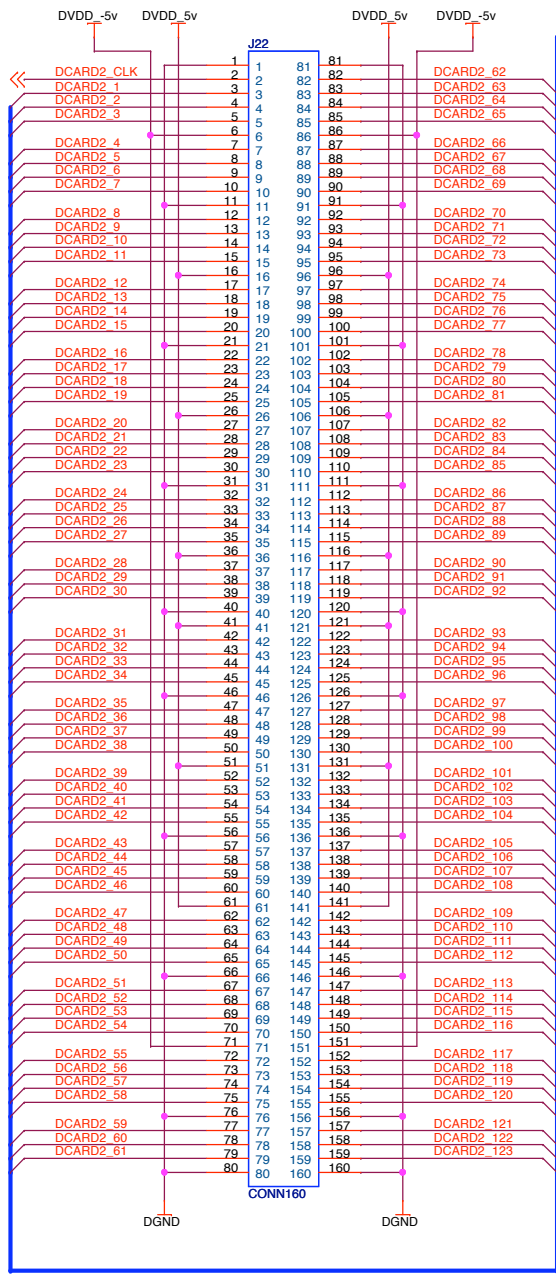


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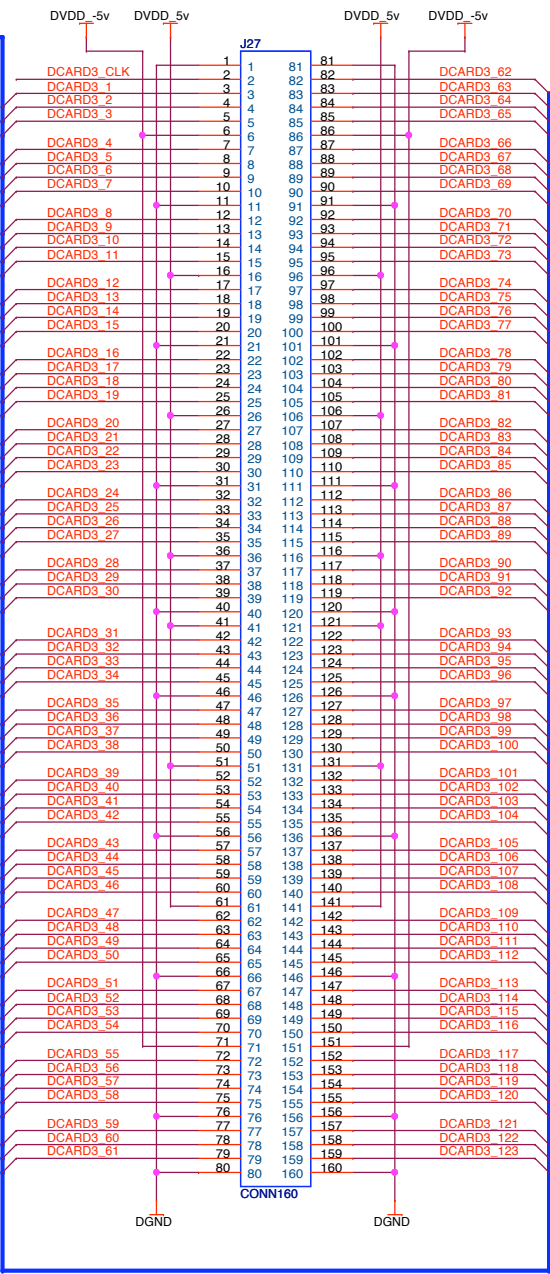


DCARD0 corresponds to Daughtercard Slot 1
 DCARD1 corresponds to Daughtercard Slot 2





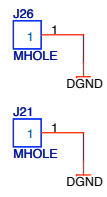
DCARD2_0

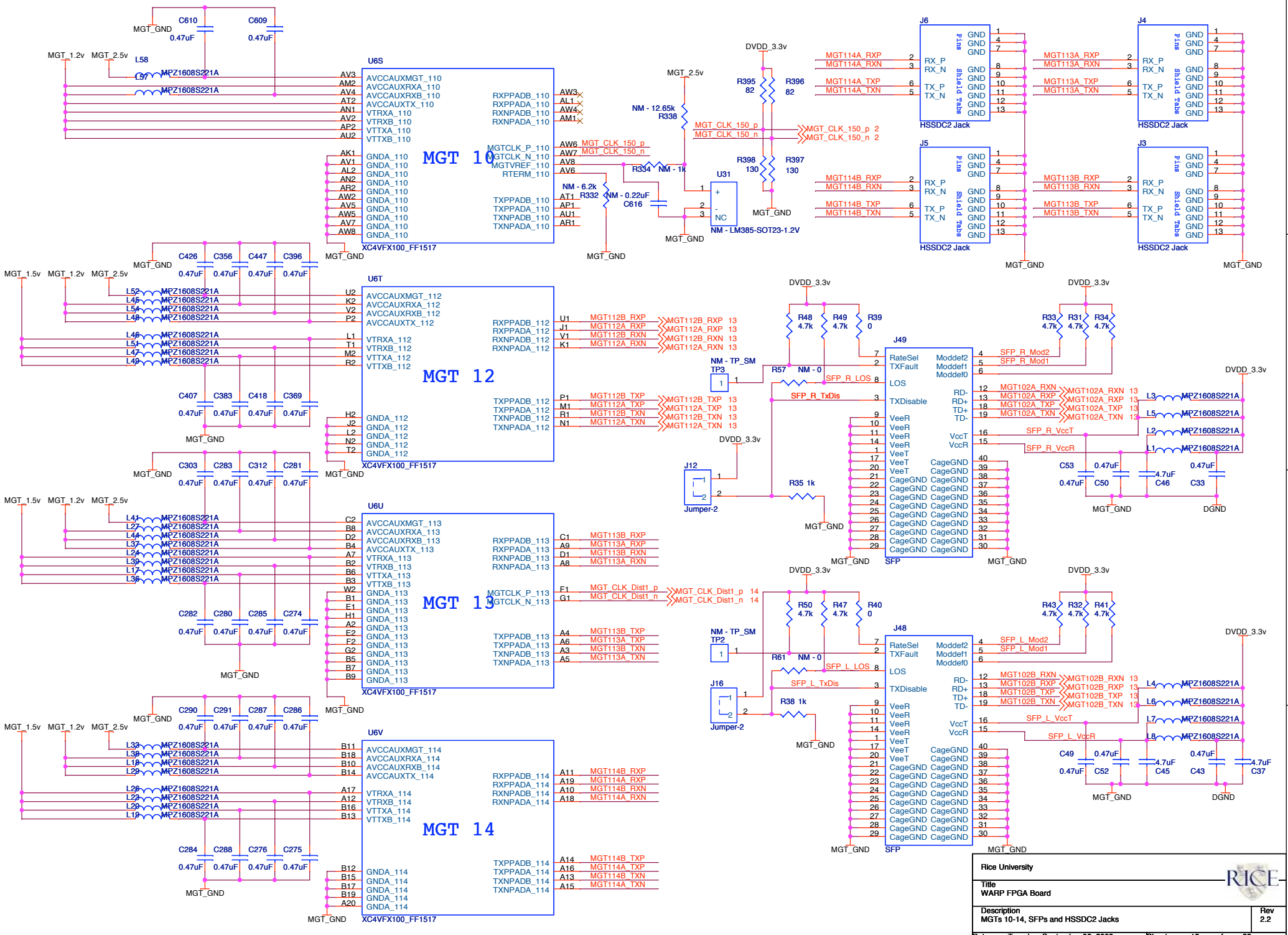


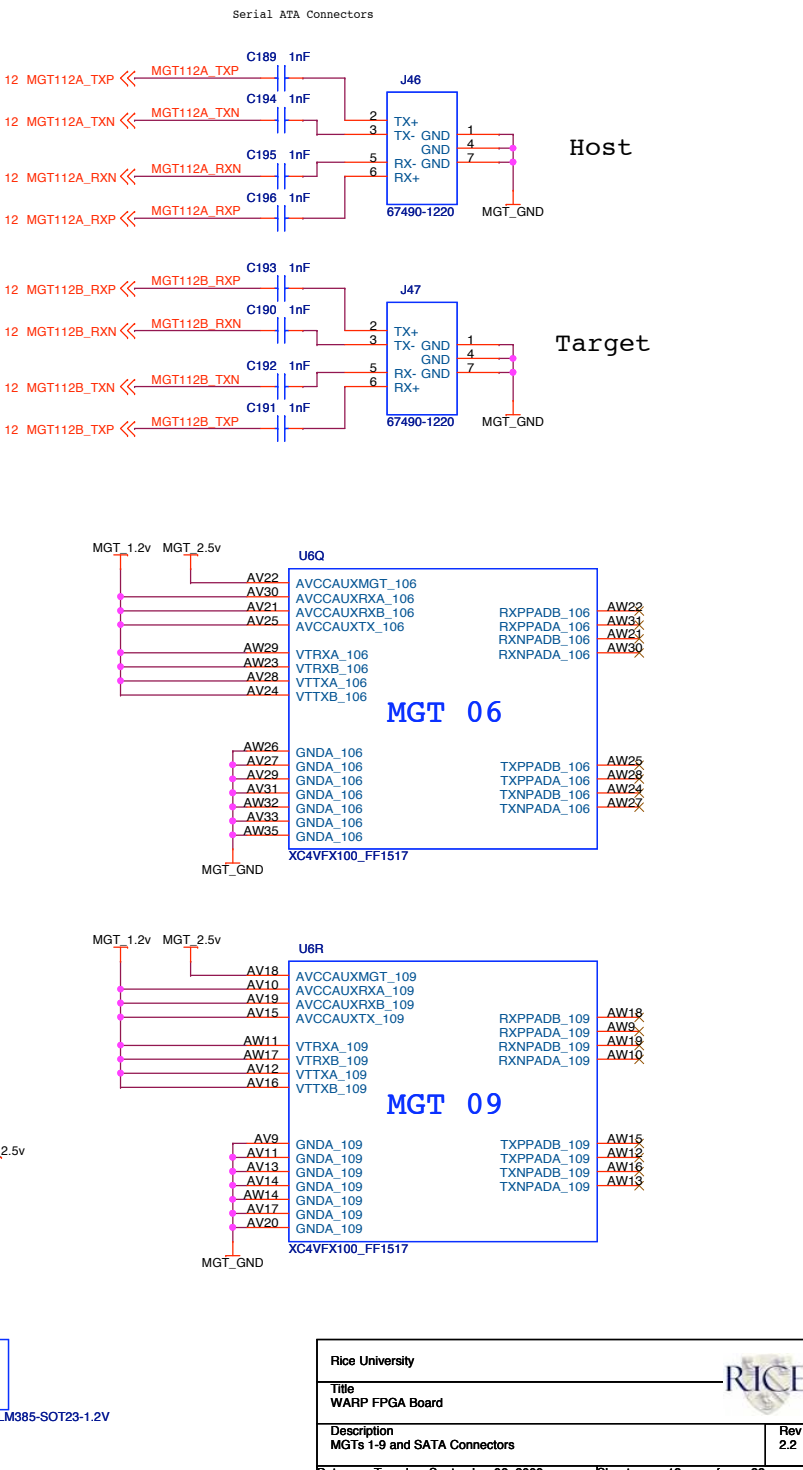
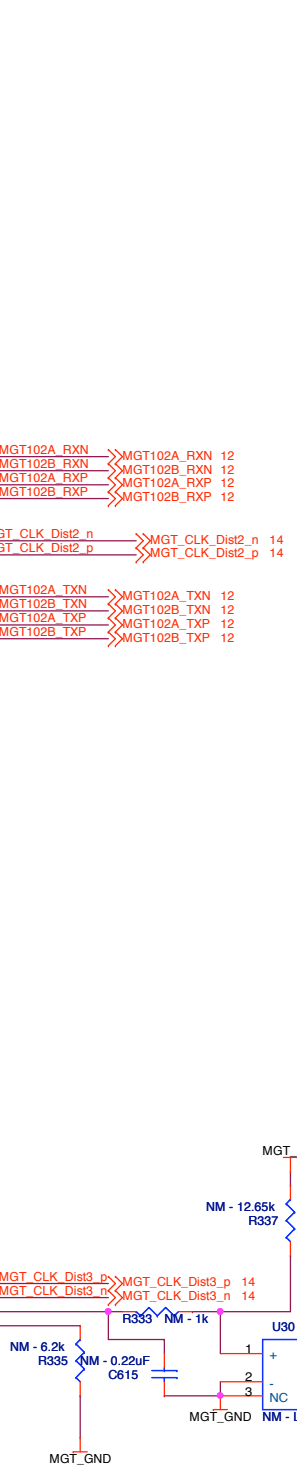
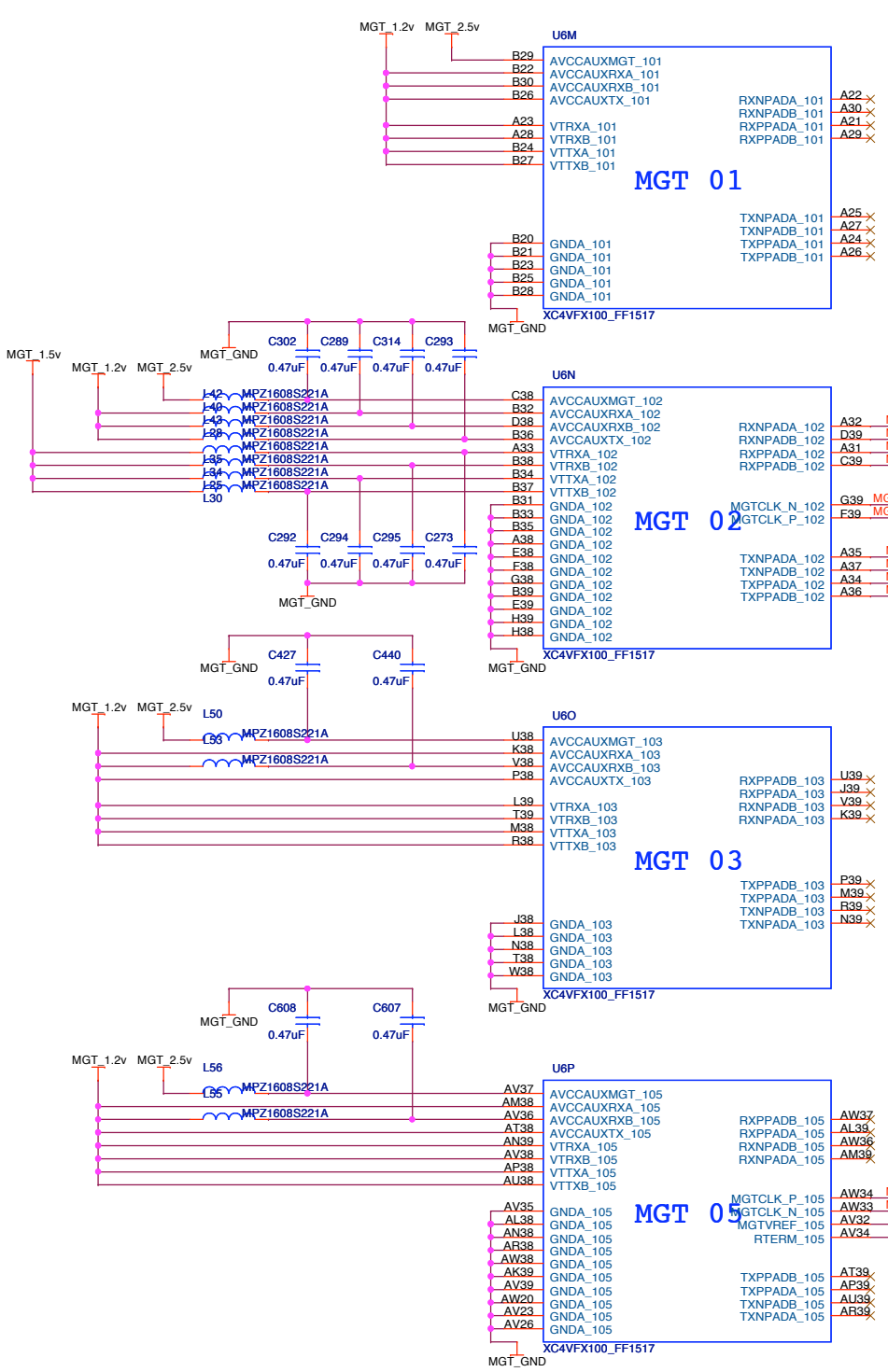
DCARD3_0

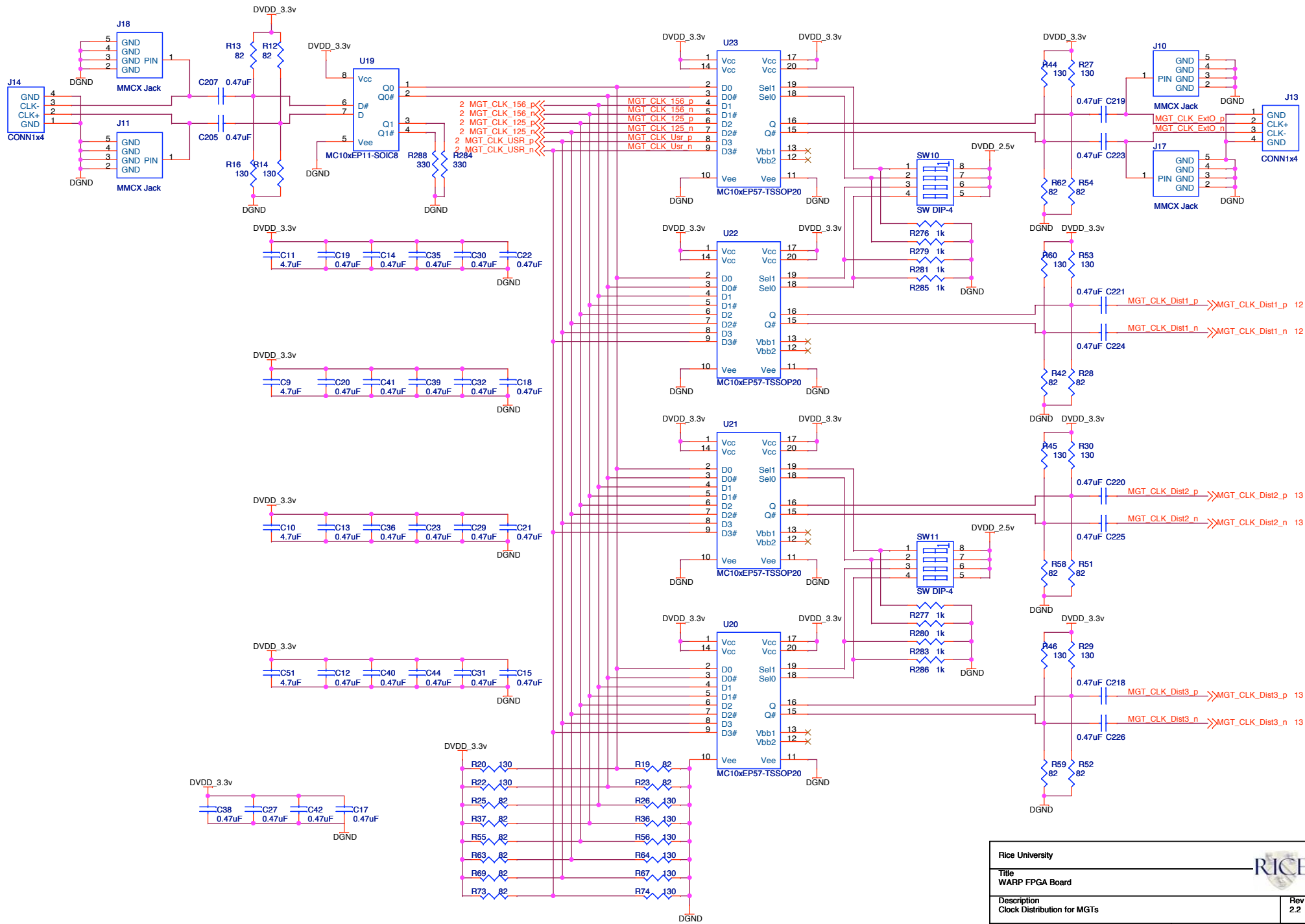
DCARD2 corresponds to Daughtercard Slot 4

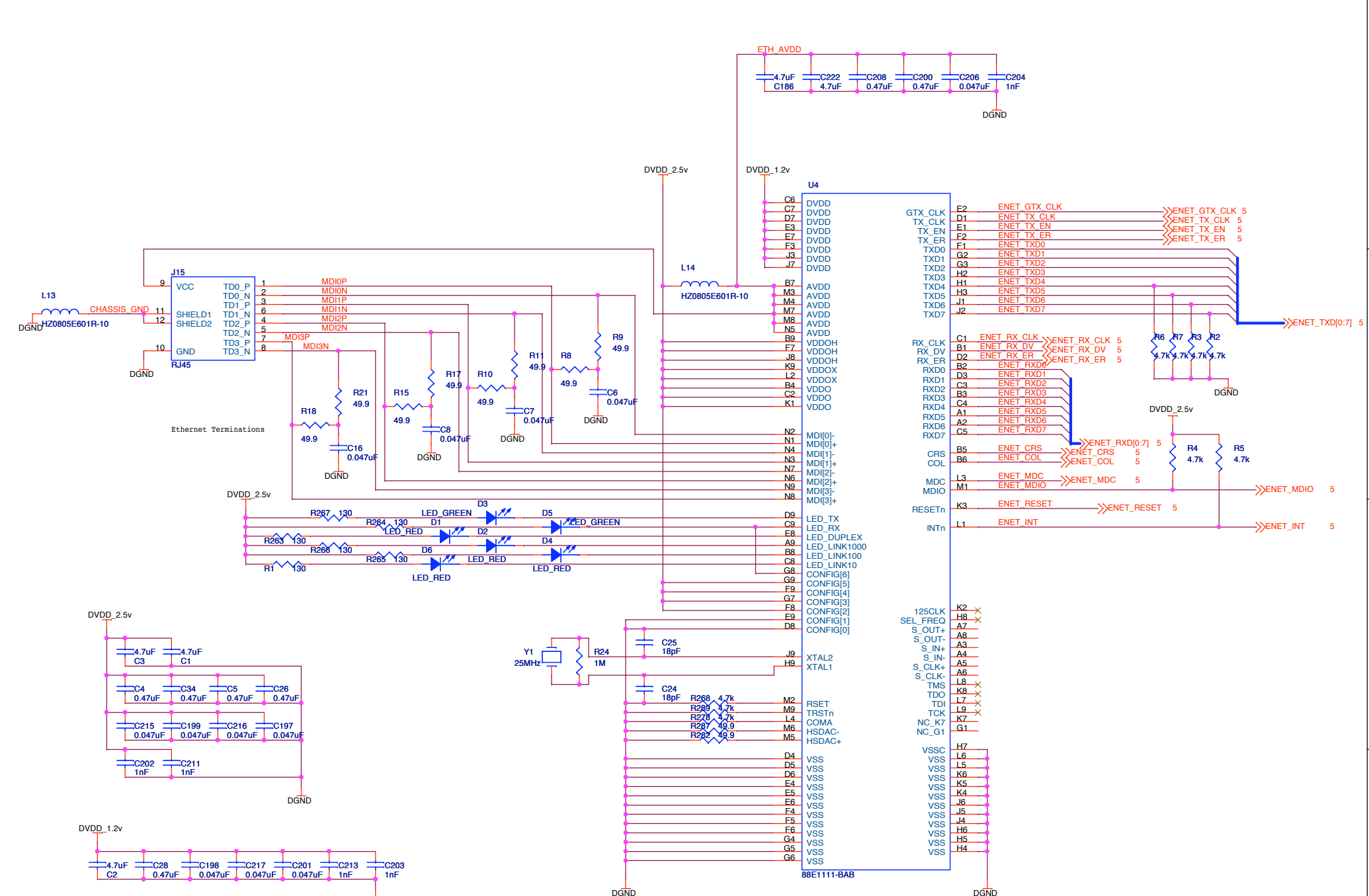
DCARD3 corresponds to Daughtercard Slot 3

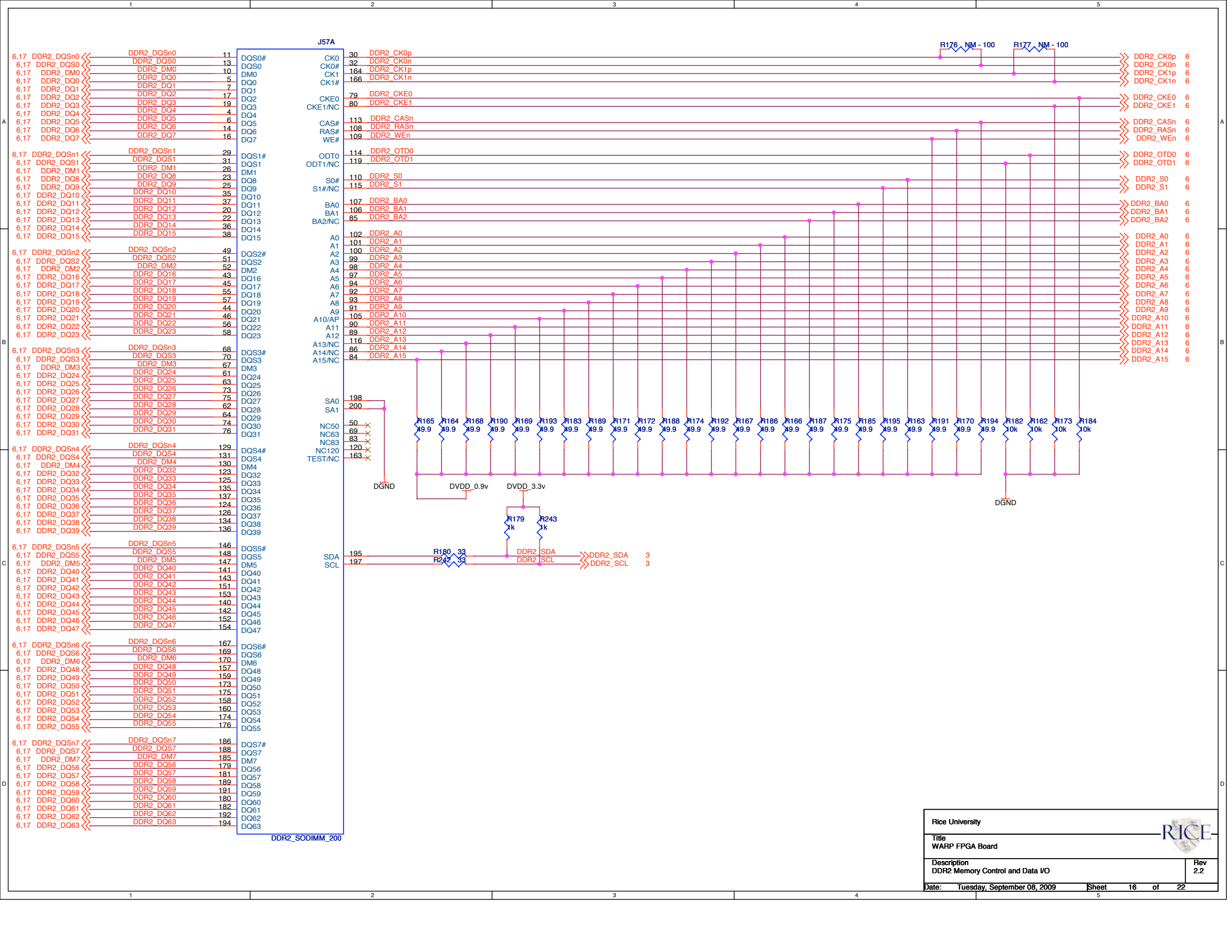








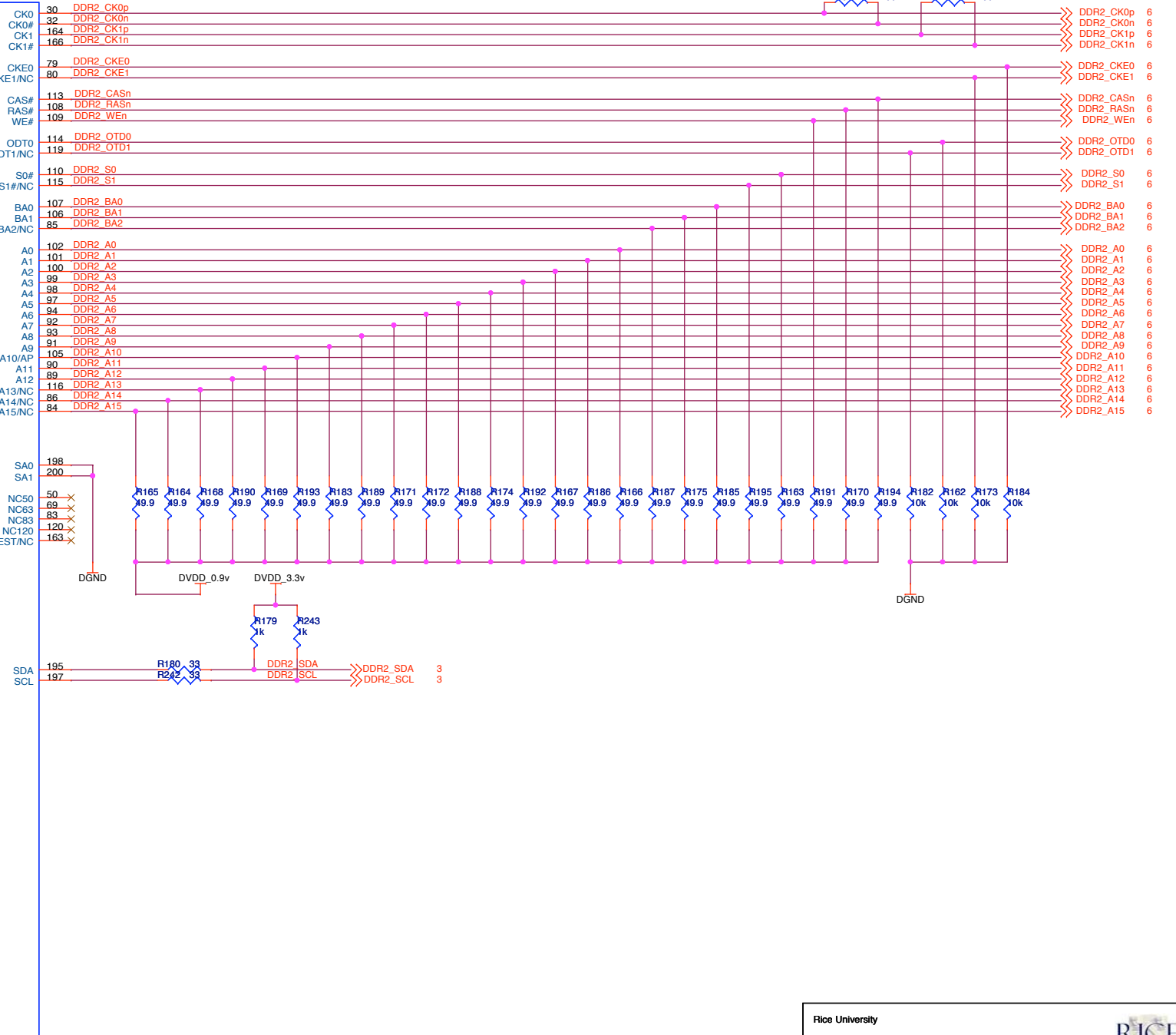




J57A

R176 NM - 100 R177 NM - 100

6,17	DDR2_DQSn0	DDR2_DQSn0	11	DQS0#
6,17	DDR2_DQ50	DDR2_DQ50	13	DQ50
6,17	DDR2_DM0	DDR2_DM0	10	DM0
6,17	DDR2_DQ0	DDR2_DQ0	5	DQ0
6,17	DDR2_DQ1	DDR2_DQ1	7	DQ1
6,17	DDR2_DQ2	DDR2_DQ2	17	DQ2
6,17	DDR2_DQ3	DDR2_DQ3	19	DQ3
6,17	DDR2_DQ4	DDR2_DQ4	4	DQ4
6,17	DDR2_DQ5	DDR2_DQ5	6	DQ5
6,17	DDR2_DQ6	DDR2_DQ6	14	DQ6
6,17	DDR2_DQ7	DDR2_DQ7	16	DQ7
6,17	DDR2_DQSn1	DDR2_DQSn1	29	DQS1#
6,17	DDR2_DQ51	DDR2_DQ51	31	DQ51
6,17	DDR2_DM1	DDR2_DM1	26	DM1
6,17	DDR2_DQ8	DDR2_DQ8	23	DQ8
6,17	DDR2_DQ9	DDR2_DQ9	25	DQ9
6,17	DDR2_DQ10	DDR2_DQ10	35	DQ10
6,17	DDR2_DQ11	DDR2_DQ11	37	DQ11
6,17	DDR2_DQ12	DDR2_DQ12	20	DQ12
6,17	DDR2_DQ13	DDR2_DQ13	22	DQ13
6,17	DDR2_DQ14	DDR2_DQ14	36	DQ14
6,17	DDR2_DQ15	DDR2_DQ15	38	DQ15
6,17	DDR2_DQSn2	DDR2_DQSn2	49	DQS2#
6,17	DDR2_DQ52	DDR2_DQ52	51	DQ52
6,17	DDR2_DM2	DDR2_DM2	52	DM2
6,17	DDR2_DQ16	DDR2_DQ16	43	DQ16
6,17	DDR2_DQ17	DDR2_DQ17	45	DQ17
6,17	DDR2_DQ18	DDR2_DQ18	55	DQ18
6,17	DDR2_DQ19	DDR2_DQ19	57	DQ19
6,17	DDR2_DQ20	DDR2_DQ20	44	DQ20
6,17	DDR2_DQ21	DDR2_DQ21	46	DQ21
6,17	DDR2_DQ22	DDR2_DQ22	56	DQ22
6,17	DDR2_DQ23	DDR2_DQ23	58	DQ23
6,17	DDR2_DQSn3	DDR2_DQSn3	68	DQS3#
6,17	DDR2_DQ53	DDR2_DQ53	70	DQ53
6,17	DDR2_DM3	DDR2_DM3	67	DM3
6,17	DDR2_DQ24	DDR2_DQ24	61	DQ24
6,17	DDR2_DQ25	DDR2_DQ25	63	DQ25
6,17	DDR2_DQ26	DDR2_DQ26	73	DQ26
6,17	DDR2_DQ27	DDR2_DQ27	75	DQ27
6,17	DDR2_DQ28	DDR2_DQ28	62	DQ28
6,17	DDR2_DQ29	DDR2_DQ29	64	DQ29
6,17	DDR2_DQ30	DDR2_DQ30	74	DQ30
6,17	DDR2_DQ31	DDR2_DQ31	76	DQ31
6,17	DDR2_DQSn4	DDR2_DQSn4	129	DQS4#
6,17	DDR2_DQ54	DDR2_DQ54	131	DQ54
6,17	DDR2_DM4	DDR2_DM4	130	DM4
6,17	DDR2_DQ32	DDR2_DQ32	123	DQ32
6,17	DDR2_DQ33	DDR2_DQ33	125	DQ33
6,17	DDR2_DQ34	DDR2_DQ34	135	DQ34
6,17	DDR2_DQ35	DDR2_DQ35	137	DQ35
6,17	DDR2_DQ36	DDR2_DQ36	124	DQ36
6,17	DDR2_DQ37	DDR2_DQ37	126	DQ37
6,17	DDR2_DQ38	DDR2_DQ38	134	DQ38
6,17	DDR2_DQ39	DDR2_DQ39	136	DQ39
6,17	DDR2_DQSn5	DDR2_DQSn5	146	DQS5#
6,17	DDR2_DQ55	DDR2_DQ55	148	DQ55
6,17	DDR2_DM5	DDR2_DM5	147	DM5
6,17	DDR2_DQ40	DDR2_DQ40	141	DQ40
6,17	DDR2_DQ41	DDR2_DQ41	143	DQ41
6,17	DDR2_DQ42	DDR2_DQ42	151	DQ42
6,17	DDR2_DQ43	DDR2_DQ43	153	DQ43
6,17	DDR2_DQ44	DDR2_DQ44	140	DQ44
6,17	DDR2_DQ45	DDR2_DQ45	142	DQ45
6,17	DDR2_DQ46	DDR2_DQ46	152	DQ46
6,17	DDR2_DQ47	DDR2_DQ47	154	DQ47
6,17	DDR2_DQSn6	DDR2_DQSn6	167	DQS6#
6,17	DDR2_DQ56	DDR2_DQ56	169	DQ56
6,17	DDR2_DM6	DDR2_DM6	170	DM6
6,17	DDR2_DQ48	DDR2_DQ48	157	DQ48
6,17	DDR2_DQ49	DDR2_DQ49	159	DQ49
6,17	DDR2_DQ50	DDR2_DQ50	173	DQ50
6,17	DDR2_DQ51	DDR2_DQ51	175	DQ51
6,17	DDR2_DQ52	DDR2_DQ52	158	DQ52
6,17	DDR2_DQ53	DDR2_DQ53	160	DQ53
6,17	DDR2_DQ54	DDR2_DQ54	174	DQ54
6,17	DDR2_DQ55	DDR2_DQ55	176	DQ55
6,17	DDR2_DQSn7	DDR2_DQSn7	186	DQS7#
6,17	DDR2_DQ57	DDR2_DQ57	188	DQ57
6,17	DDR2_DM7	DDR2_DM7	185	DM7
6,17	DDR2_DQ56	DDR2_DQ56	179	DQ56
6,17	DDR2_DQ57	DDR2_DQ57	181	DQ57
6,17	DDR2_DQ58	DDR2_DQ58	189	DQ58
6,17	DDR2_DQ59	DDR2_DQ59	191	DQ59
6,17	DDR2_DQ60	DDR2_DQ60	180	DQ60
6,17	DDR2_DQ61	DDR2_DQ61	182	DQ61
6,17	DDR2_DQ62	DDR2_DQ62	192	DQ62
6,17	DDR2_DQ63	DDR2_DQ63	194	DQ63



DDR2_SODIMM_200

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Rev 2.2

