


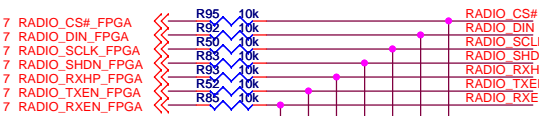
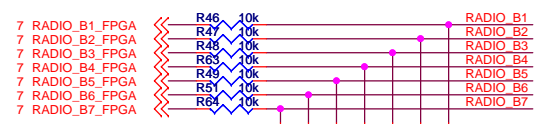
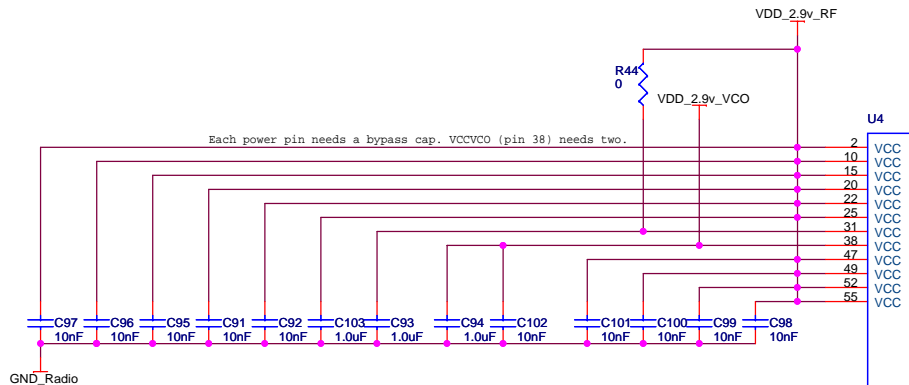
WARP Radio Board

MAX2829 Version - Rev x3

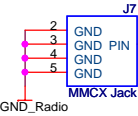
Schematic Pages:

- 1 - Table of Contents
- 2 - MAX2829 RF Transceiver
- 3 - Rx A/D Converter
- 4 - Tx D/A Converter
- 5 - RSSI A/D Converter
- 6 - RF Front End
- 7 - FPGA Board Headers
- 8 - Clocks & Power

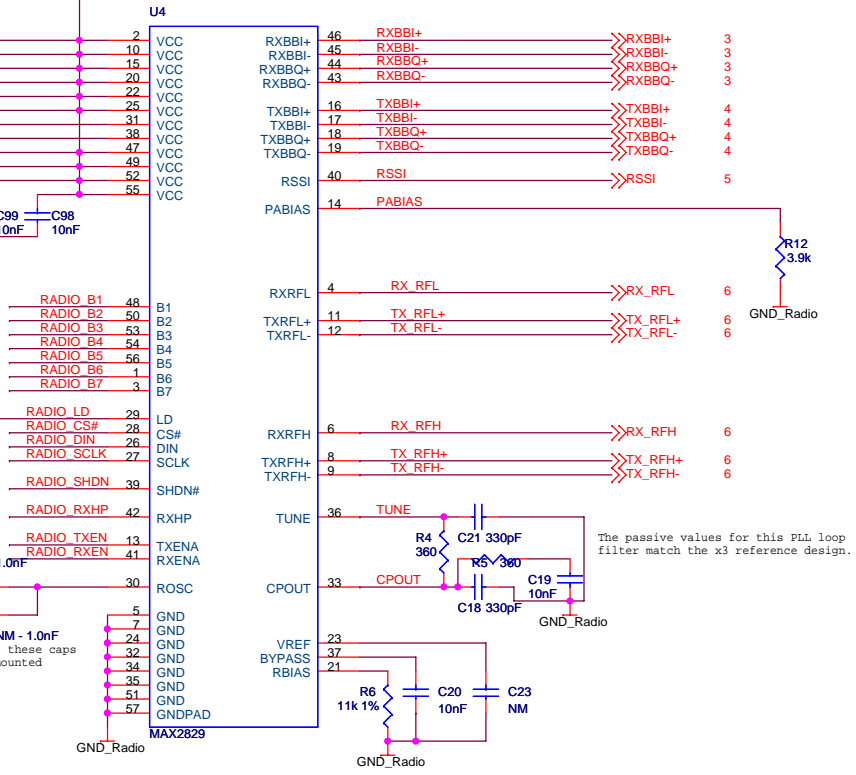
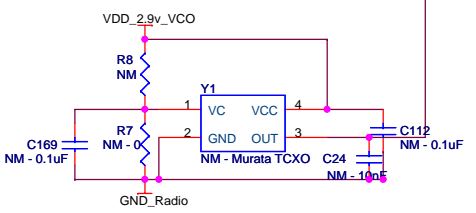
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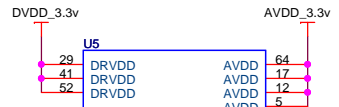
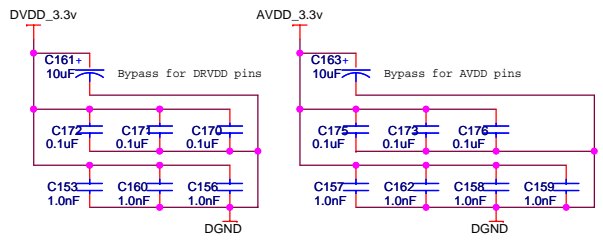
7 RADIO_LD <<<
 LD is an output in [0,2.9]v
 2.9v is above Vih for the FPGA
 when Vcco=3.3v, so no explicit
 level shifting is required.



Signals driven from FPGA to MAX2829 Inputs
 need to be scaled to [0,2.9]v from [0,3.3]v and
 are current limited.
 See pg. 5 of MAX2825 design guide.

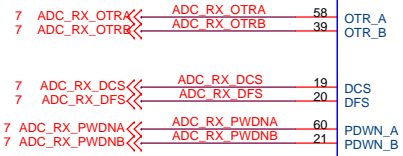
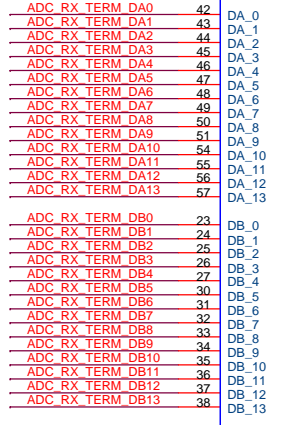
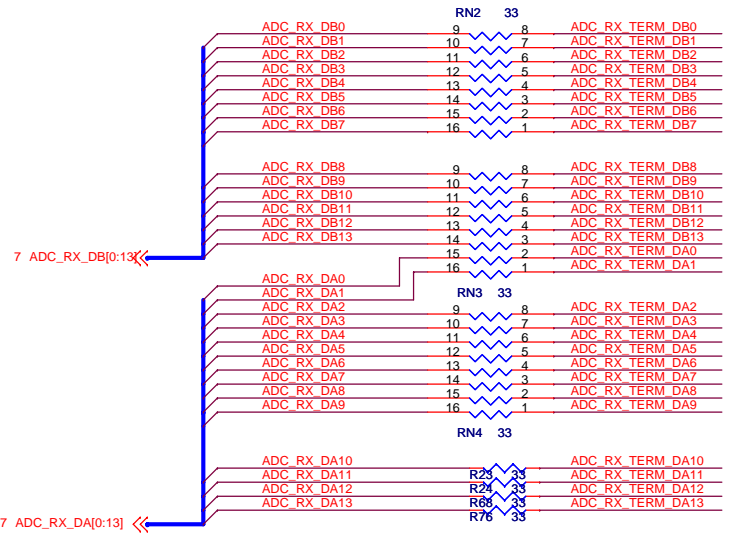


The passive values for this PLL loop
 filter match the x3 reference design.

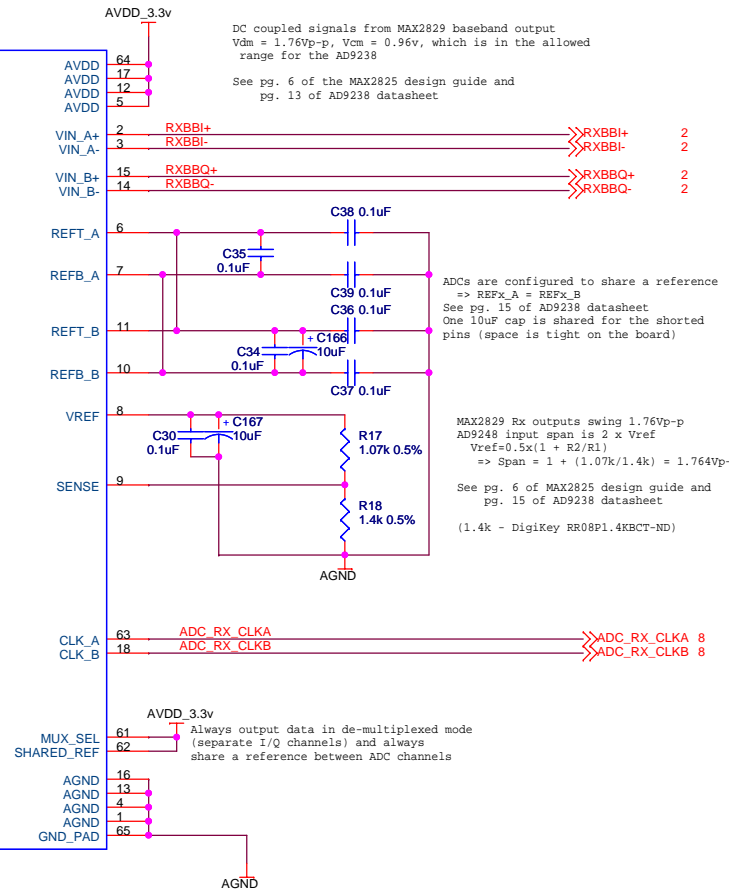


DC coupled signals from MAX2829 baseband output
 $V_{dm} = 1.76V_{p-p}$, $V_{cm} = 0.96V$, which is in the allowed range for the AD9238

See pg. 6 of the MAX2825 design guide and pg. 13 of AD9238 datasheet



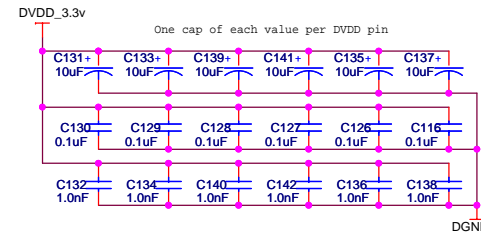
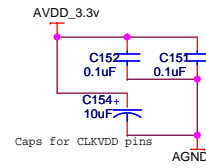
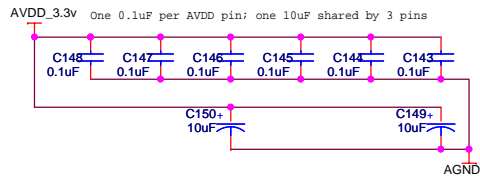
Outputs always enabled. FPGA can use PDWN to disable chip and just ignore the data outputs.



ADCs are configured to share a reference
 $\Rightarrow REF_A = REF_B$
 See pg. 15 of AD9238 datasheet
 One 10uF cap is shared for the shorted pins (space is tight on the board)

MAX2829 Rx outputs swing 1.76Vp-p
 AD9248 input span is $2 \times V_{ref}$
 $V_{ref} = 0.5 \times (1 + R_2/R_1)$
 $\Rightarrow \text{Span} = 1 + (1.07k/1.4k) = 1.764V_{p-p}$
 See pg. 6 of MAX2825 design guide and pg. 15 of AD9238 datasheet
 (1.4k - DigiKey RR08P1.4KBCT-ND)

AVDD_3.3v
 Always output data in de-multiplexed mode (separate I/Q channels) and always share a reference between ADC channels



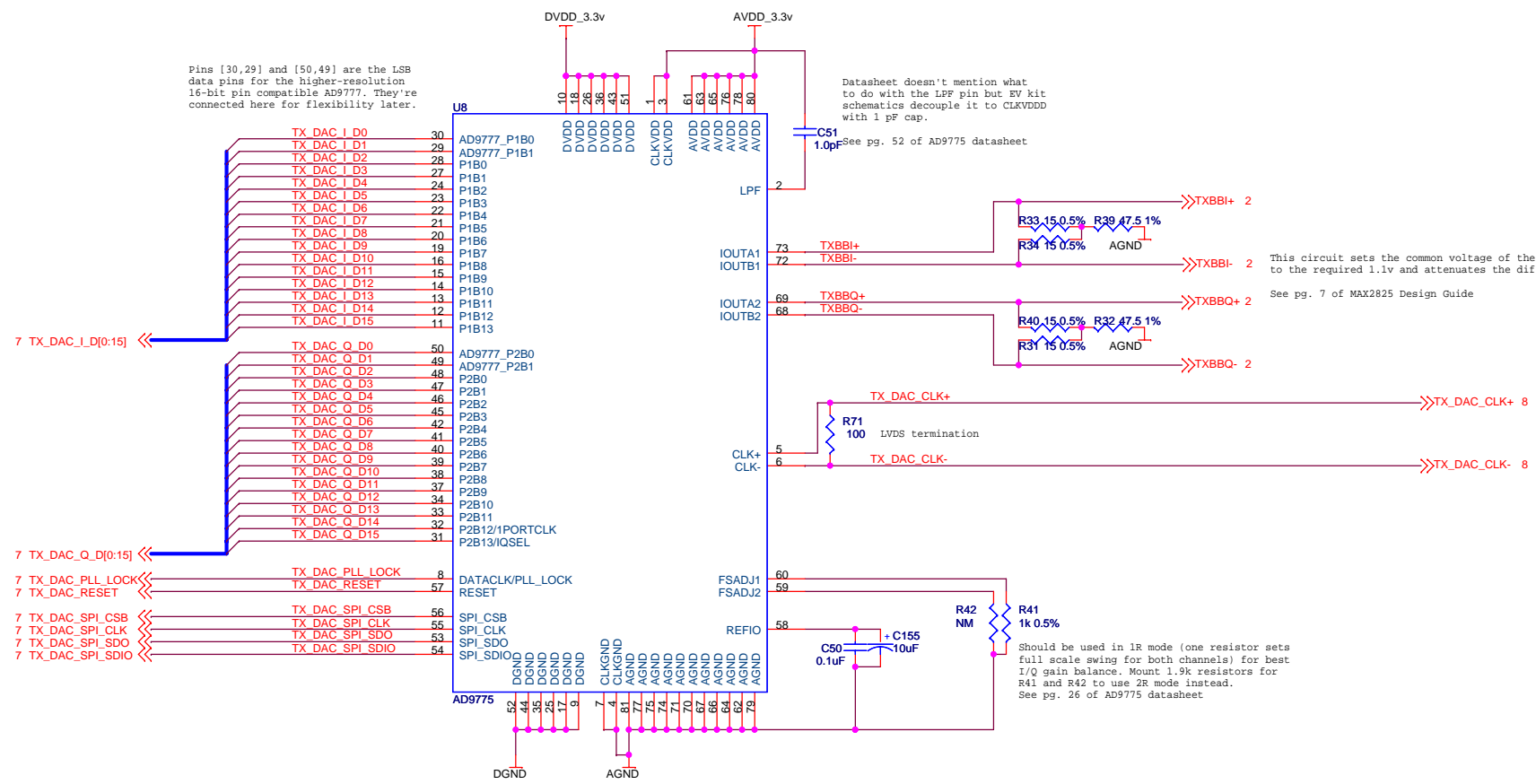
Pins [30,29] and [50,49] are the LSB data pins for the higher-resolution 16-bit pin compatible AD9777. They're connected here for flexibility later.

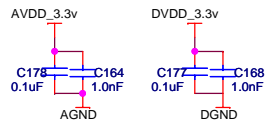
Datasheet doesn't mention what to do with the LPF pin but EV kit schematics decouple it to CLKVDD with 1 pF cap.

See pg. 52 of AD9775 datasheet

This circuit sets the common voltage of the differential signals to the required 1.1v and attenuates the diff swing to around 100mVrms
See pg. 7 of MAX2825 Design Guide

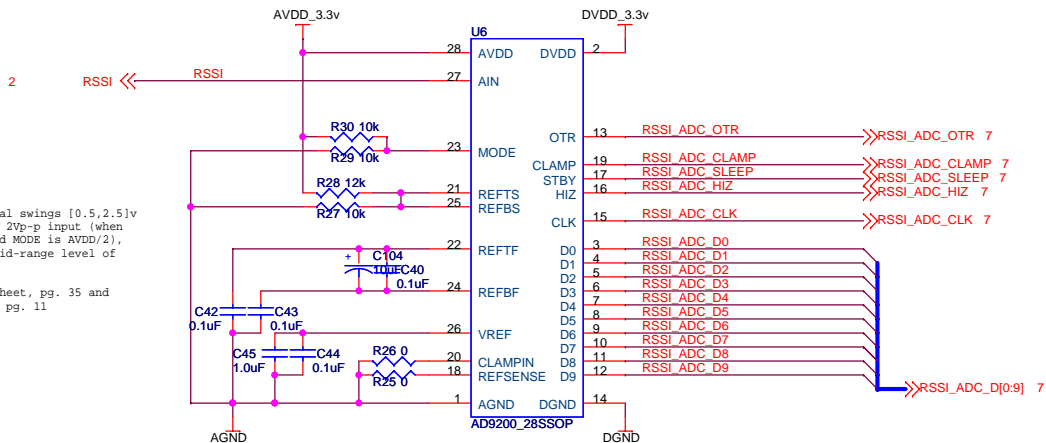
Should be used in 1R mode (one resistor sets full scale swing for both channels) for best 1/Q gain balance. Mount 1.9k resistors for R41 and R42 to use 2R mode instead.
See pg. 26 of AD9775 datasheet

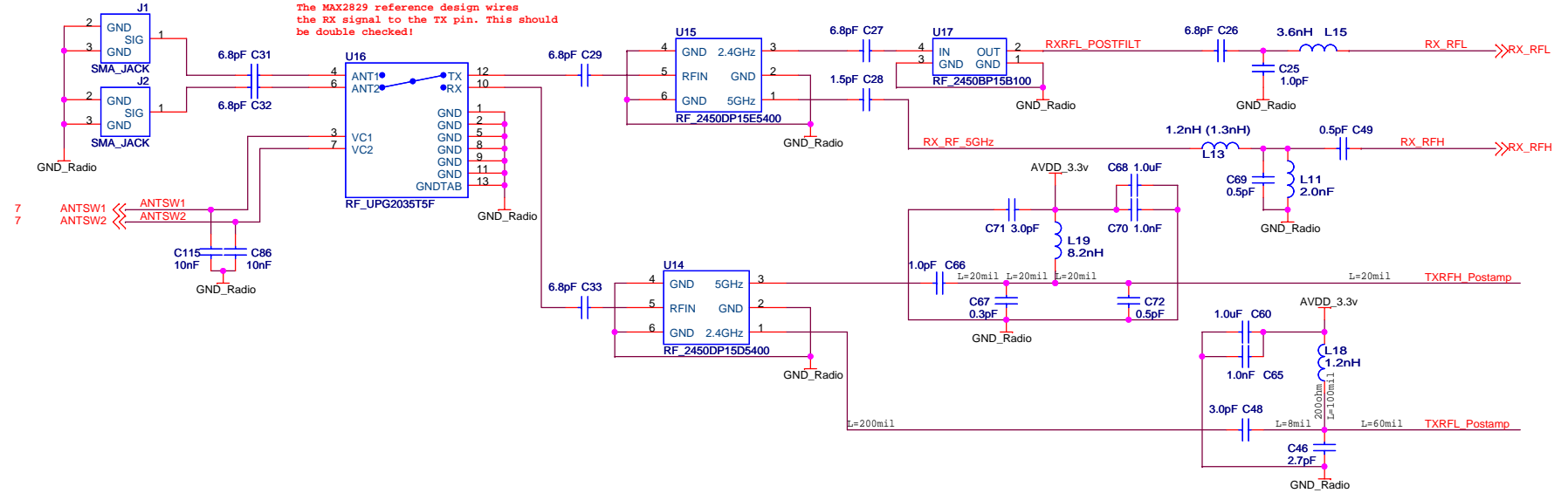




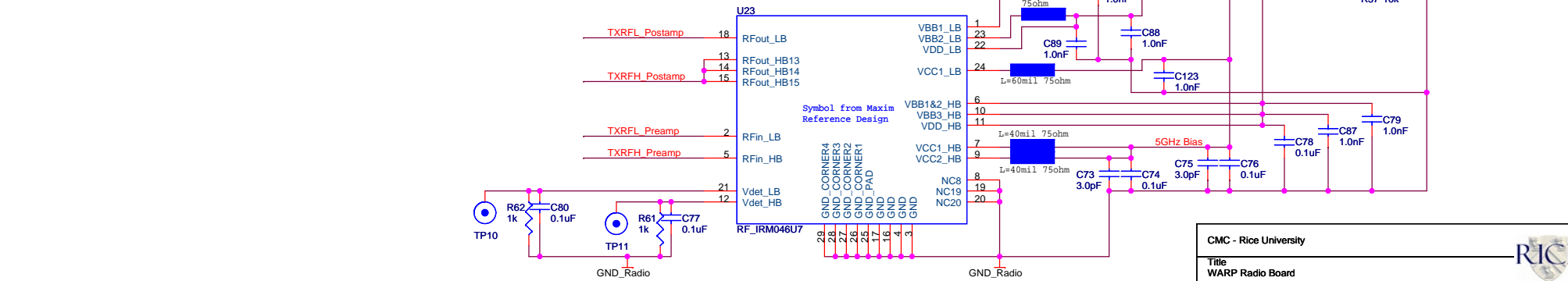
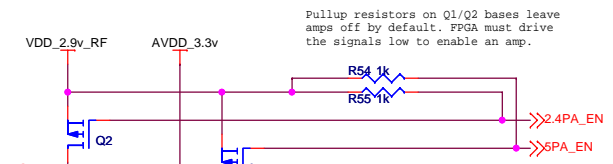
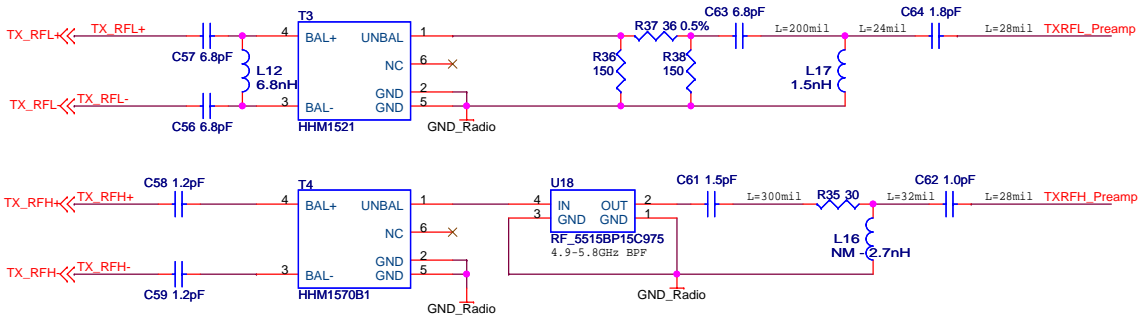
MAX2829 RSSI signal swings [0.5,2.5]v
 AD9200 supports a 2Vp-p input (when
 REFSENSE is 0v and MODE is AVDD/2),
 so this needs a mid-range level of
 1.5v=REFTS=REFBS.

See MAX2829 datasheet, pg. 35 and
 AD9200 datasheet, pg. 11

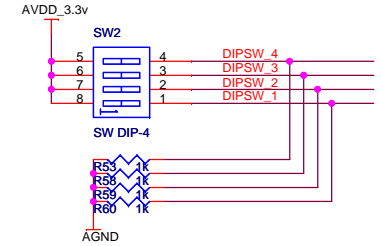
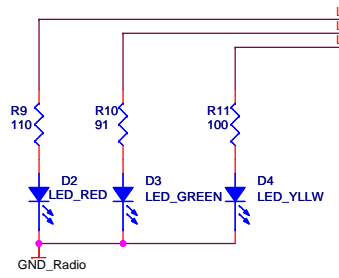
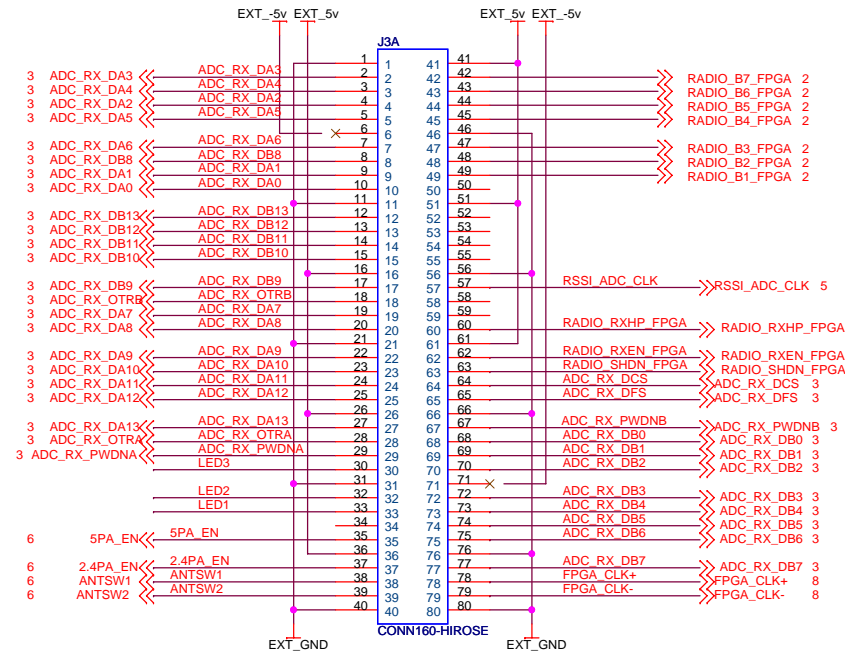
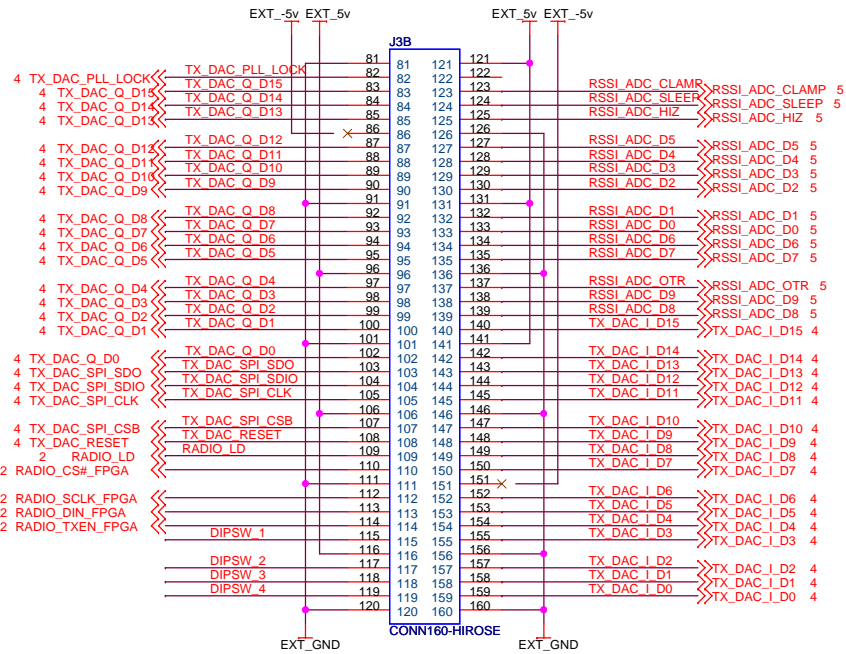


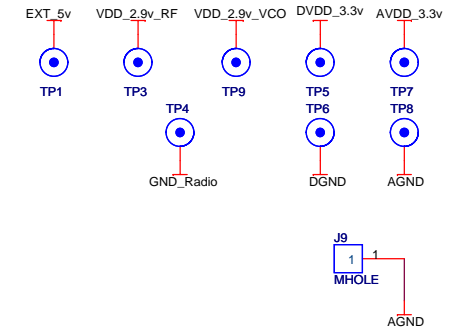
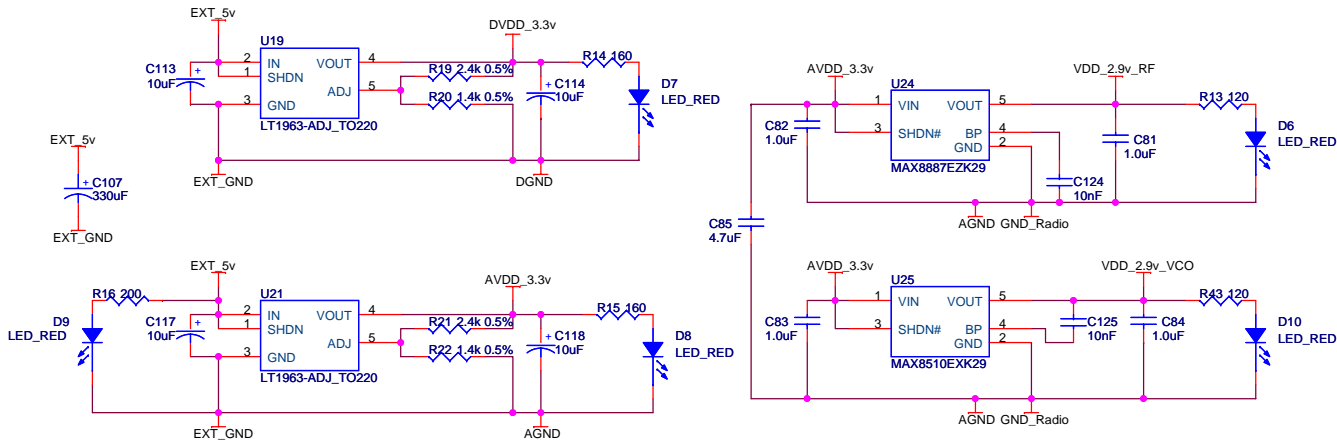


EVKit uses TDK Baluns, which are available from Digikey. The MAX2829 ref design uses Murata baluns, which are harder to get. These are the TDK parts with I/O impedances and passive values matched to the latest ref design.



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Mount these resistors to allow the FPGA to drive the clock input for the data converters. These *must* be removed to use the external clock connector.

