


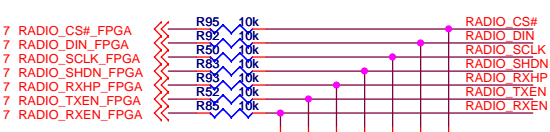
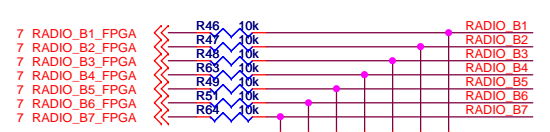
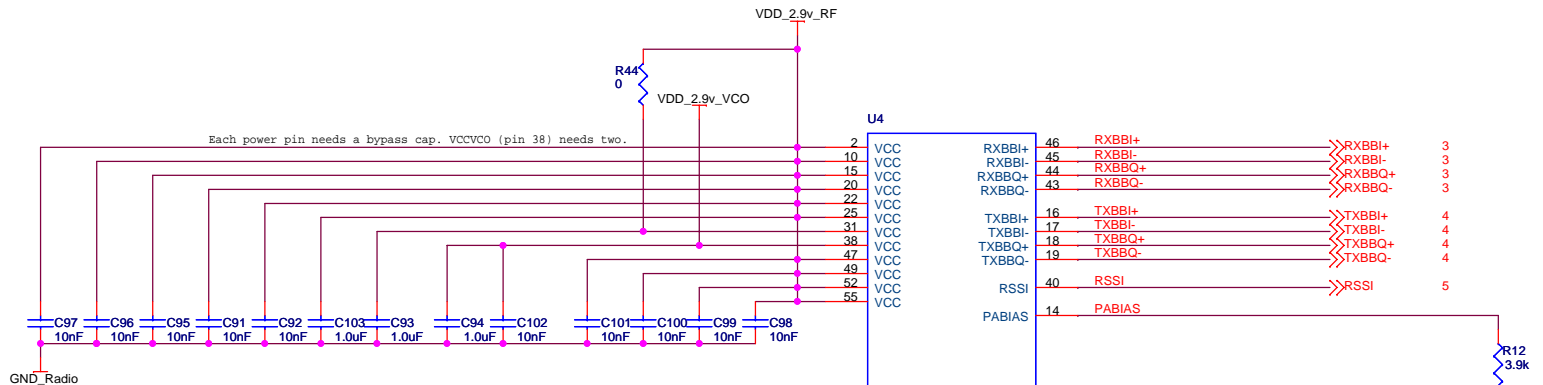
WARP Radio Board

MAX2829 Version - Rev 1.4

Schematic Pages:

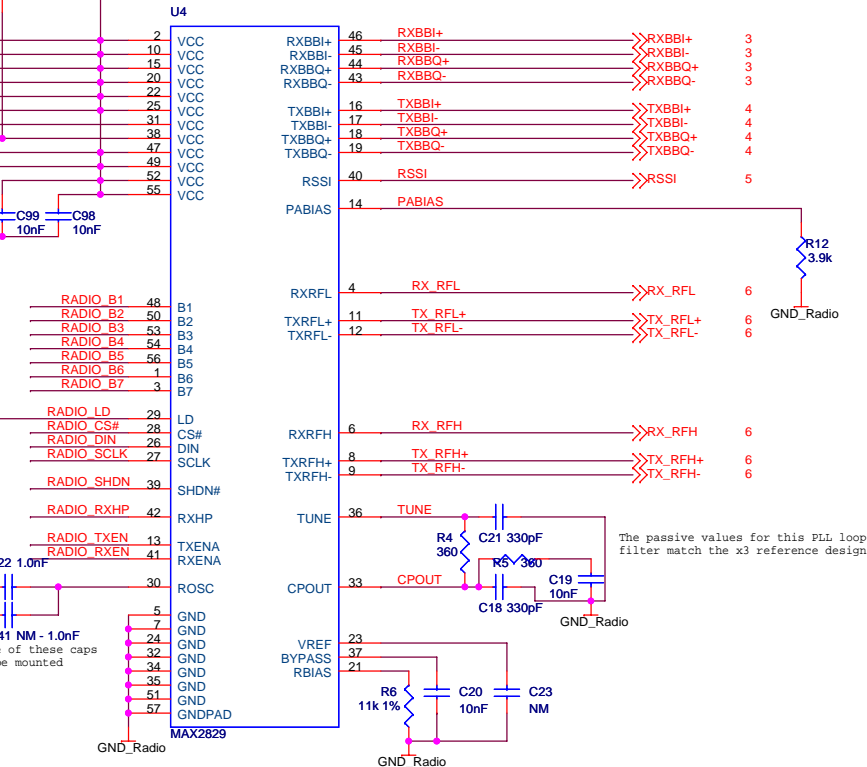
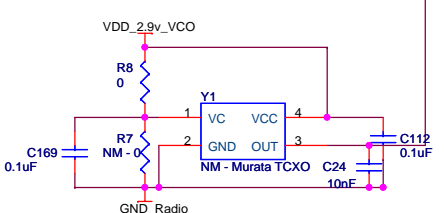
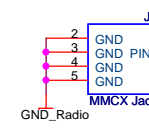
- 1 - Table of Contents
- 2 - MAX2829 RF Transceiver
- 3 - Rx A/D Converter
- 4 - Tx D/A Converter
- 5 - RSSI A/D Converter
- 6 - RF Front End
- 7 - FPGA Board Headers
- 8 - Clocks & Power

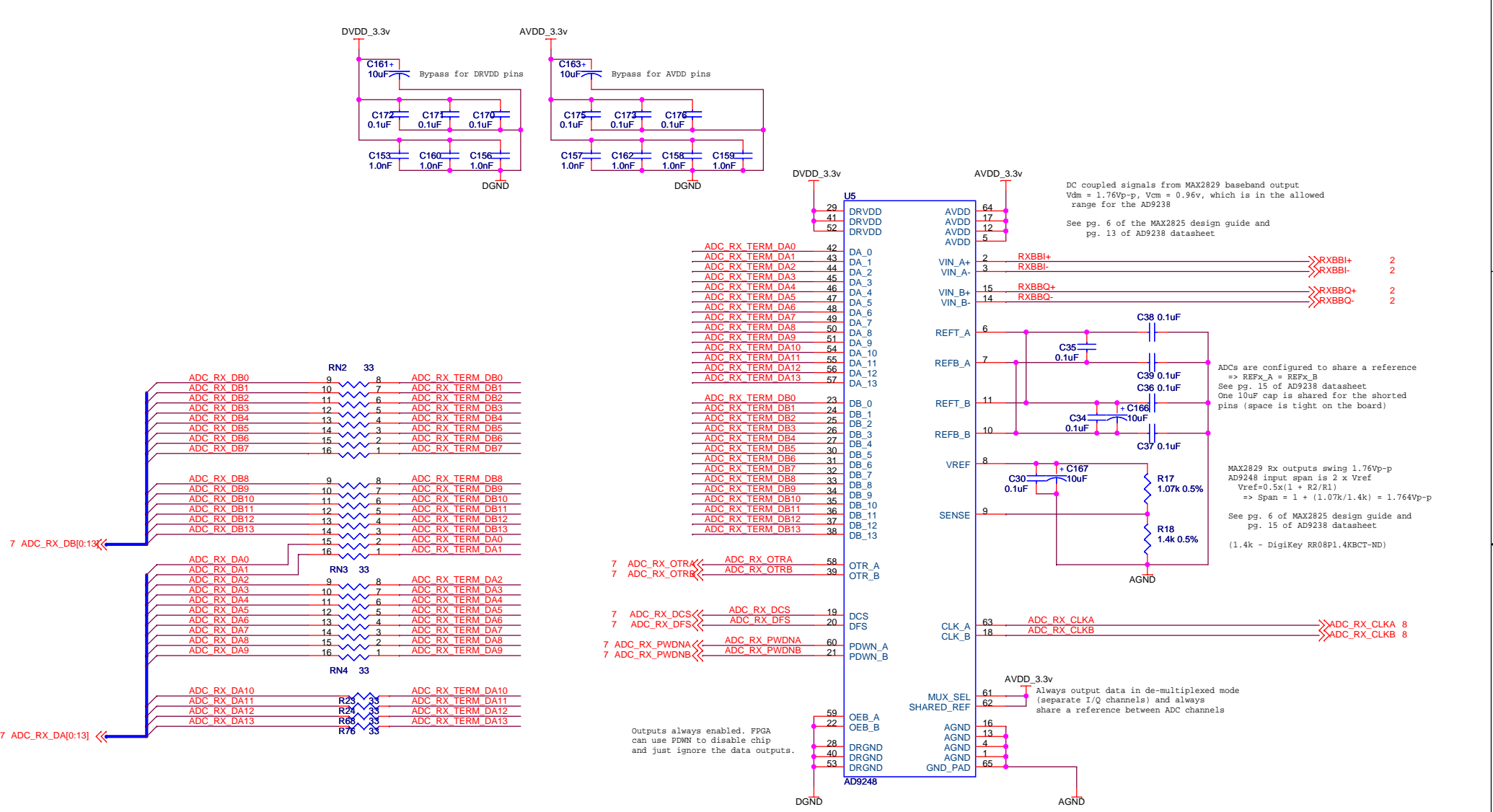
CMC - Rice University		
Title WARP Radio Board		
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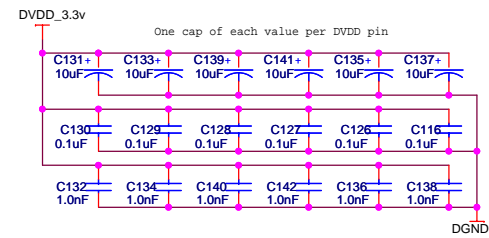
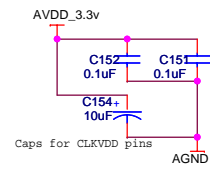
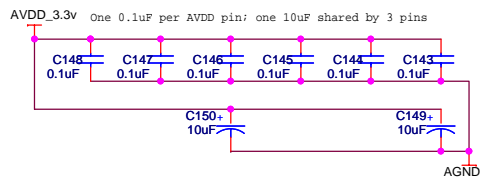


7 RADIO_LD <<<
 LD is an output in [0,2.9]v
 2.9v is above Vih for the FPGA
 when Vcco=3.3v, so no explicit
 level shifting is required.

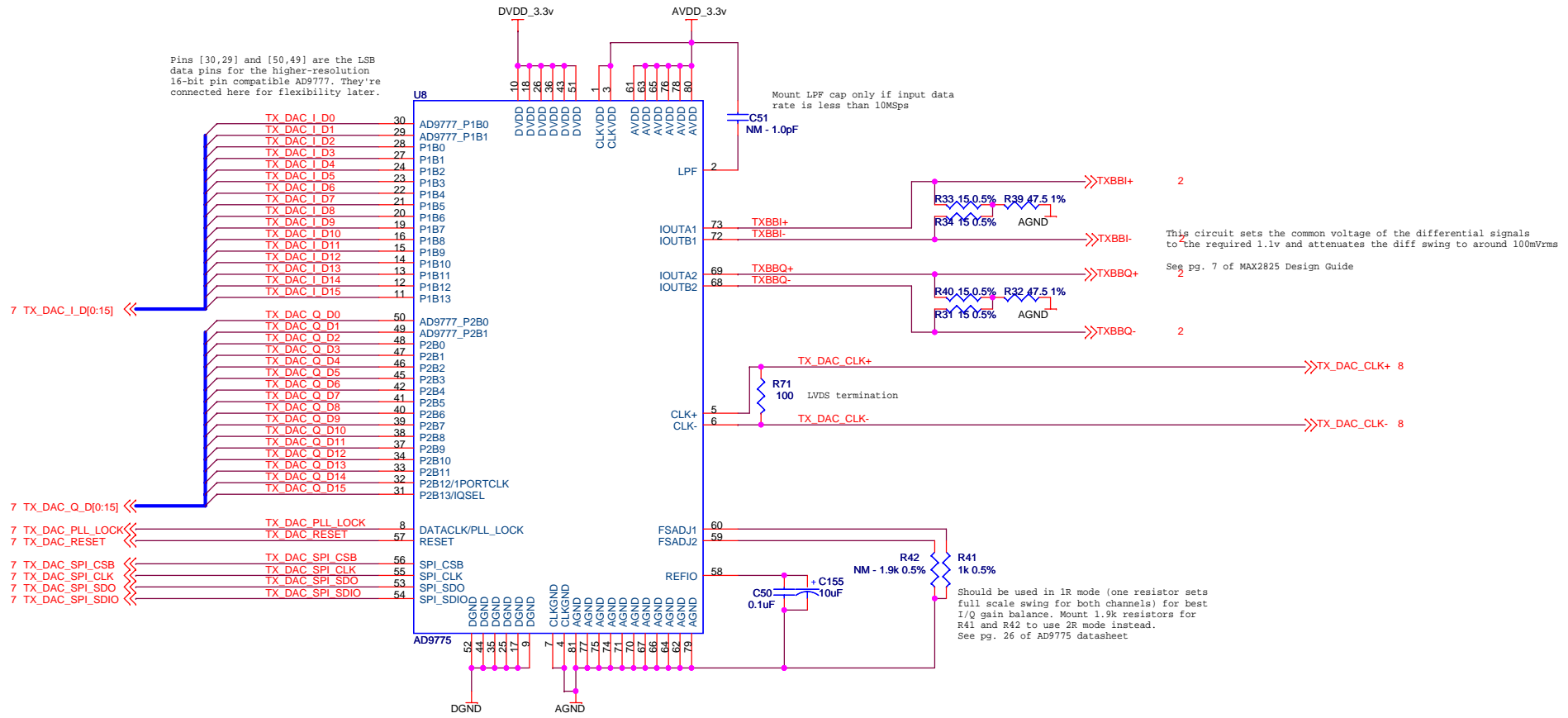
Signals driven from FPGA to MAX2829 Inputs
 need to be scaled to [0,2.9]v from [0,3.3]v and
 be current limited.
 See pg. 5 of MAX2825 design guide.

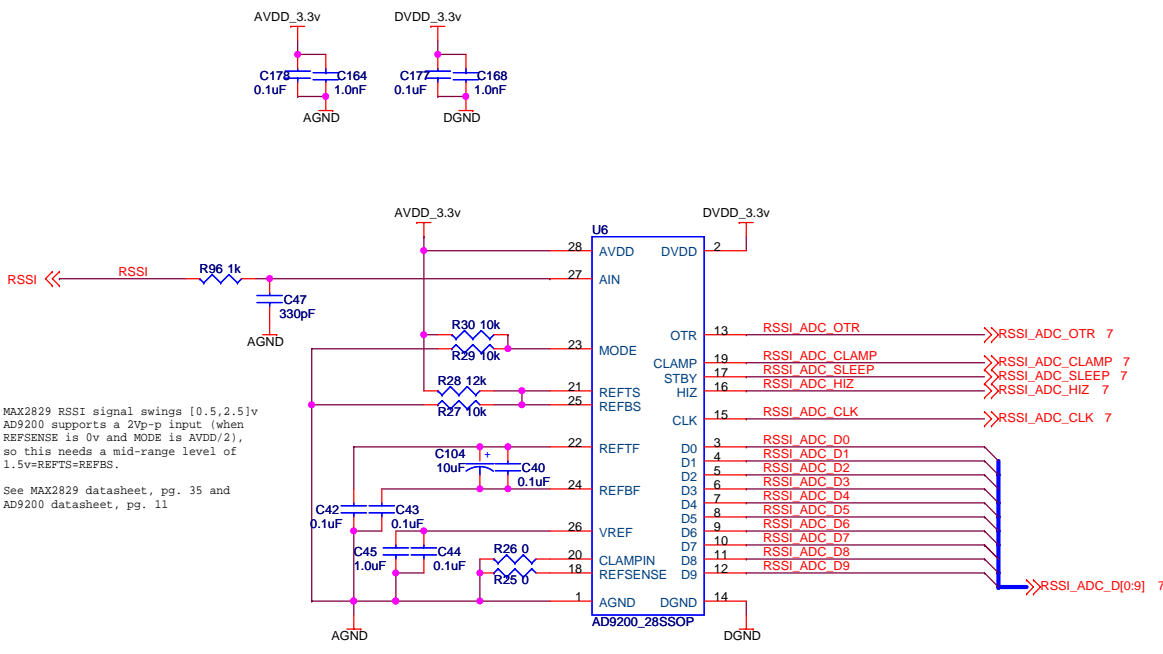







Pins [30,29] and [50,49] are the LSB data pins for the higher-resolution 16-bit pin compatible AD9777. They're connected here for flexibility later.

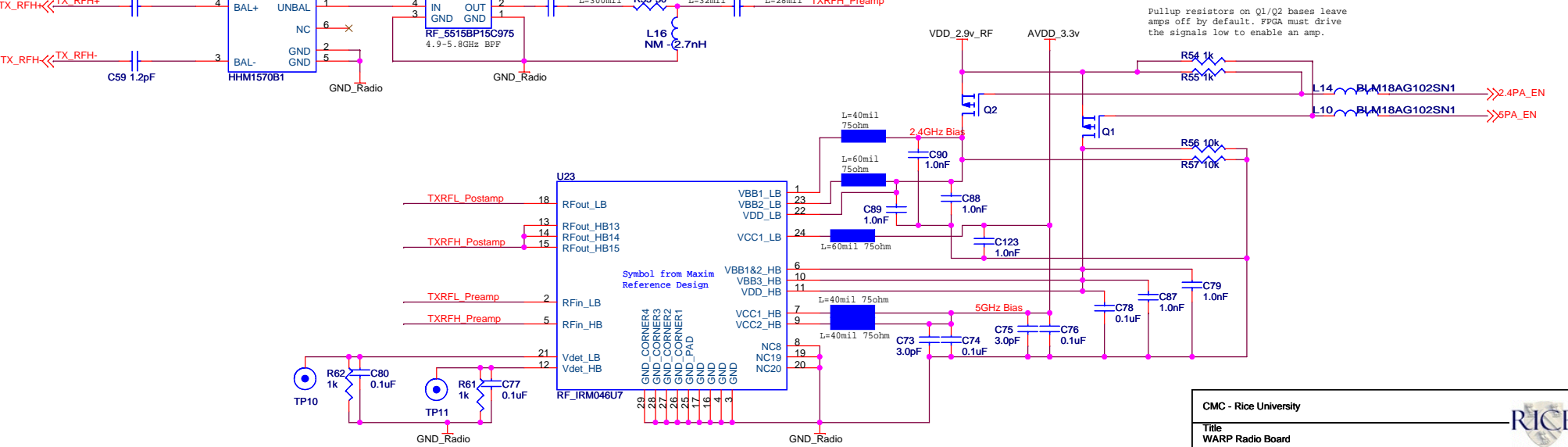
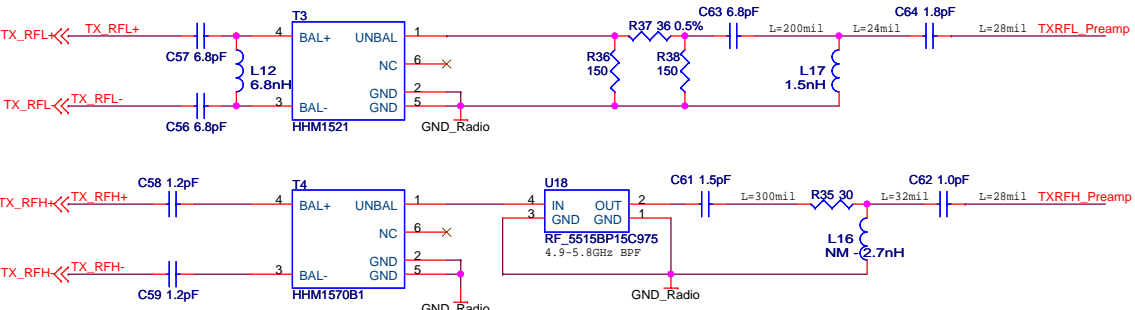
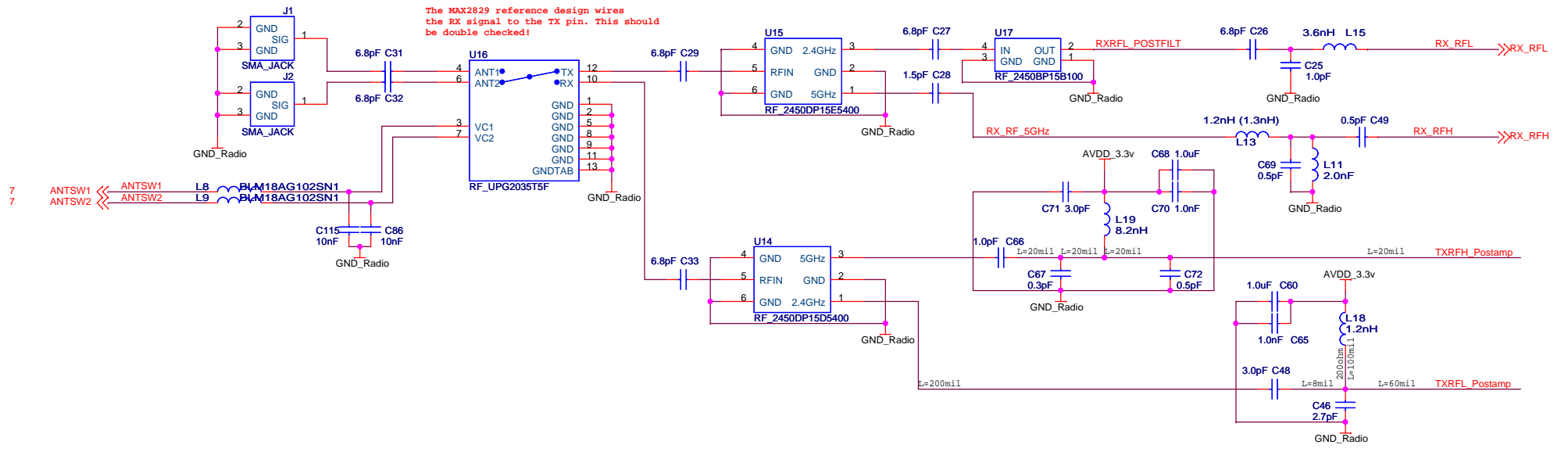


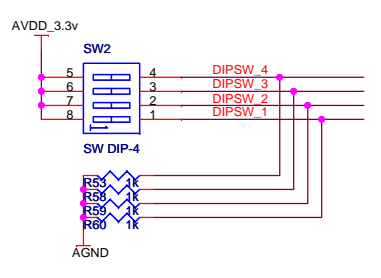
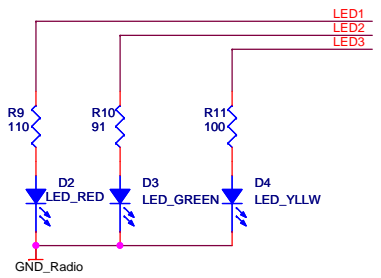
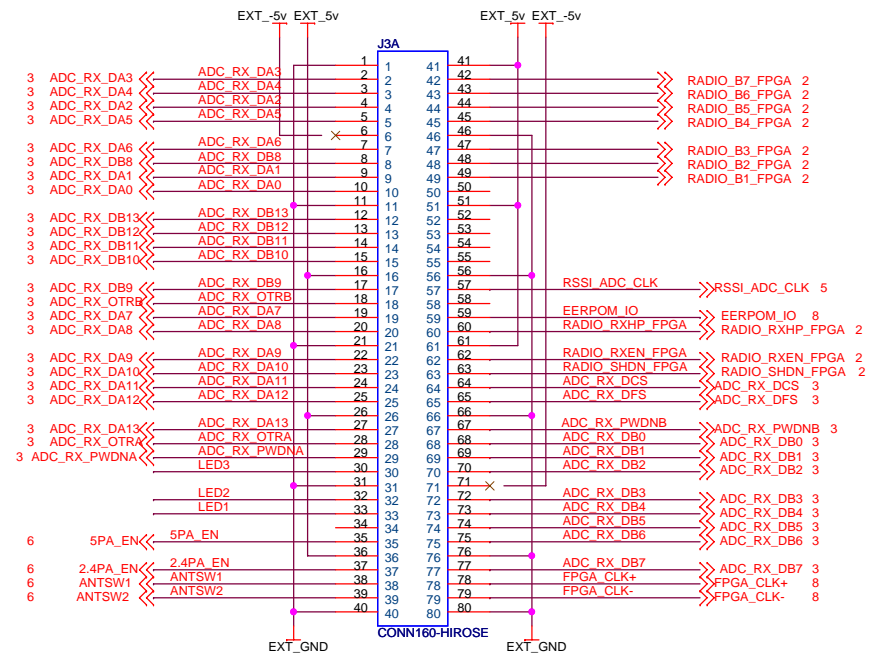
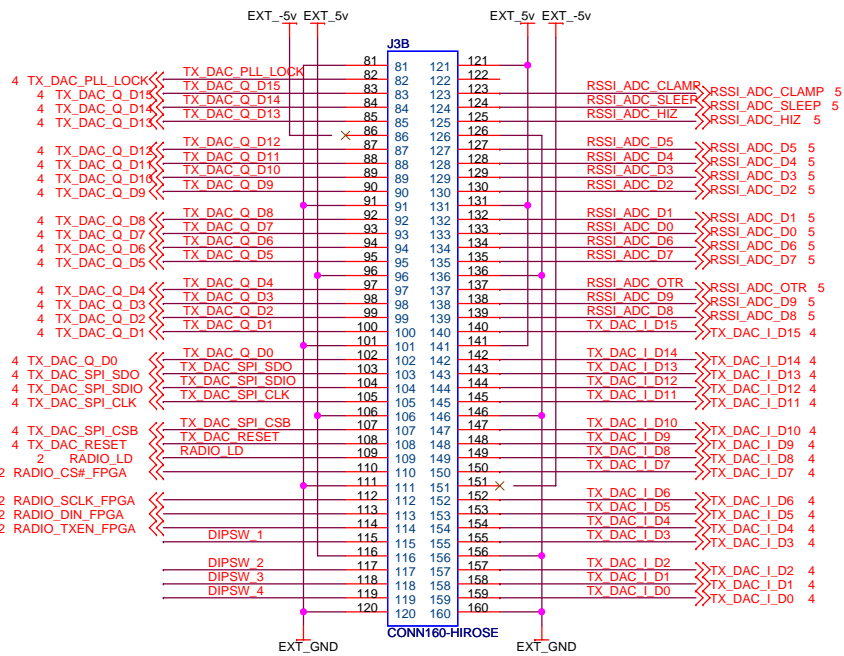


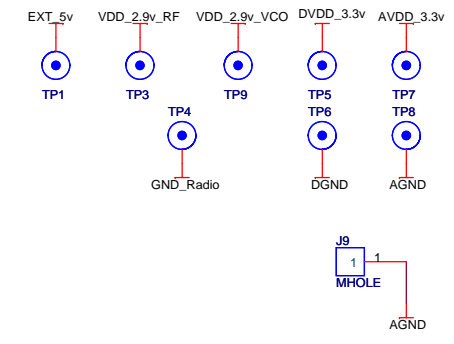
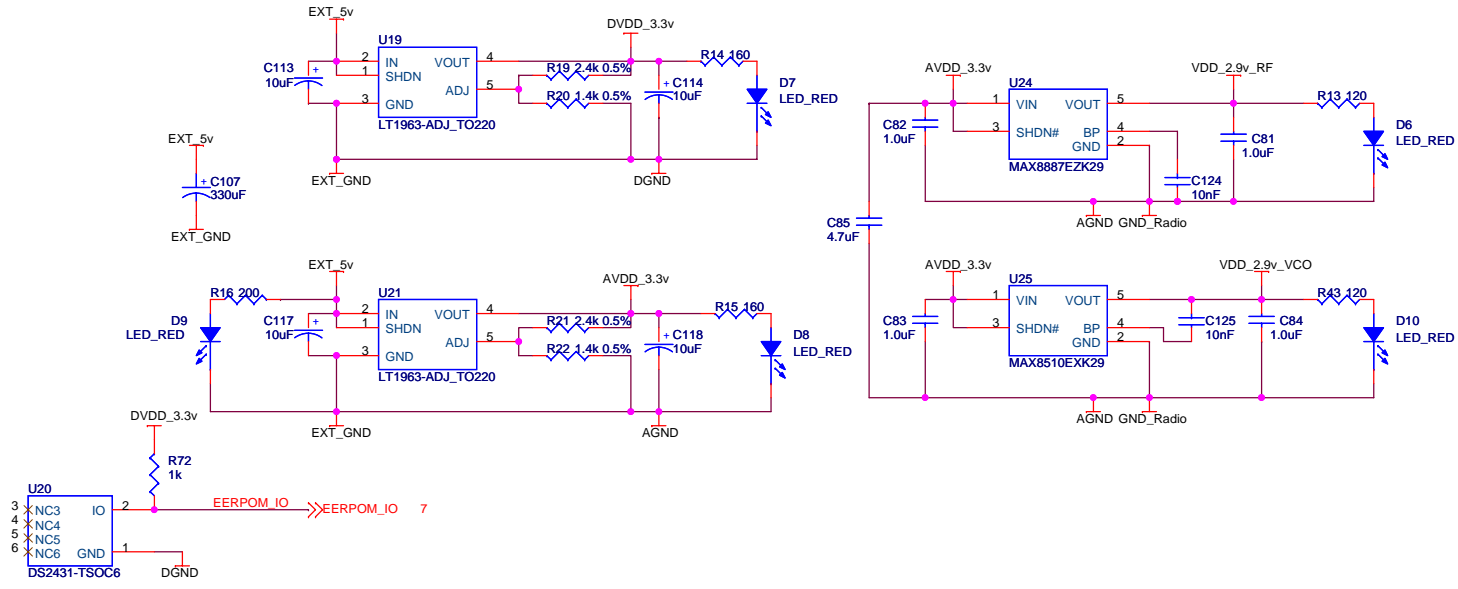
MAX2829 RSSI signal swings [0.5,2.5]v
 AD9200 supports a 2Vp-p input (when
 REFSENSE is 0v and MODE is AVDD/2),
 so this needs a mid-range level of
 1.5v=REFTS=REFBS.

See MAX2829 datasheet, pg. 35 and
 AD9200 datasheet, pg. 11

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Mount these resistors to allow the FPGA to drive the clock input for the data converters. These *must* be removed to use the external clock connector.

