WIRELESS OPEN-ACCESS
RESEARCH PLATFORM

WARP FPGA Board User I/O Reference Design

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1 Connecting and Powering the WARP FGPA Board

1.1 Hardware Requirements

- Power Supply for the WARP FPGA Board (12V-DC)
- Parallel Cable w/ JTAG (Requires 5V-DC supply for Xilinx Parallel Cable IV)
- 9-pin serial cable

1.2 Connecting the Board

1.2.1 Connect and Power the Parallel Cable

1. Attach the parallel cable to the 25-pin port on your computer.
2. Attach the parallel cable to the board using the JTAG connector. (The connection to the board is underneath the board on the middle-left side)
3. Connect the parallel cable to a 5V-DC power supply. (The status light on the parallel cable should be yellow before the board is powered)

1.2.2 Connect the Serial Cable

1. Attach the 9-pin serial cable to one of the COM ports of your computer
2. Attach the serial cable to the board. (The connection to the board is in the lower right hand corner on the right side of the board)

1.2.3 Connect and Power the WARP FPGA Board

1. Connect a 12V-DC power supply to the FPGA board. (The connection to the board is in the bottom right corner on the bottom side)
2. Turn the power switch on. The switch is located to the left of the power connection. (Turning on the board should cause a number of LEDs to light. If there is no flash card in the flash port, then the LED near the flash port will blink until one is inserted. This is not needed now.)

2 Setting up the Project in XPS

2.1 Create New Project

1. Start XPS via **Program Files** → **Xilinx Platform Studio 8.1i** → **Xilinx Platform Studio**
2. At the **Create new or open existing project** window, select **Base System Builder** wizard (recommended) and click **OK**

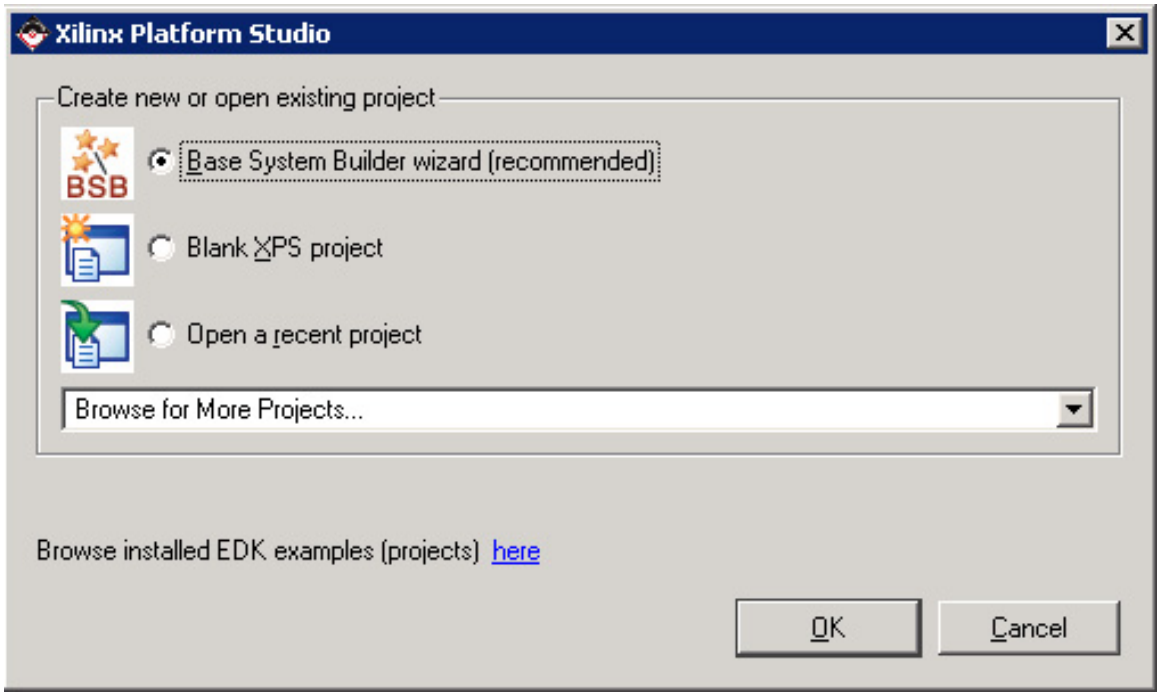

Figure 1: Step 2 – Opening Dialog Box

3. For **Project file**, Either:
   (a) Enter: **C:/WARP/BoardTests/IOTest/system.xmp**.
   Click **OK** and click **Yes** when asked if you would like to create the directory; OR
   (b) Browse to the directory in which you would like to store your project. Create a new folder within this directory and open it. The file name should be system.xmp. Click **Save**. XPS will save all the various project files and folders in this project folder. Click **OK** to move to tthe next window.
   (c) This readme assumes method one when giving locations. You must adjust your addresses accordingly if choosing to save the system elsewhere.

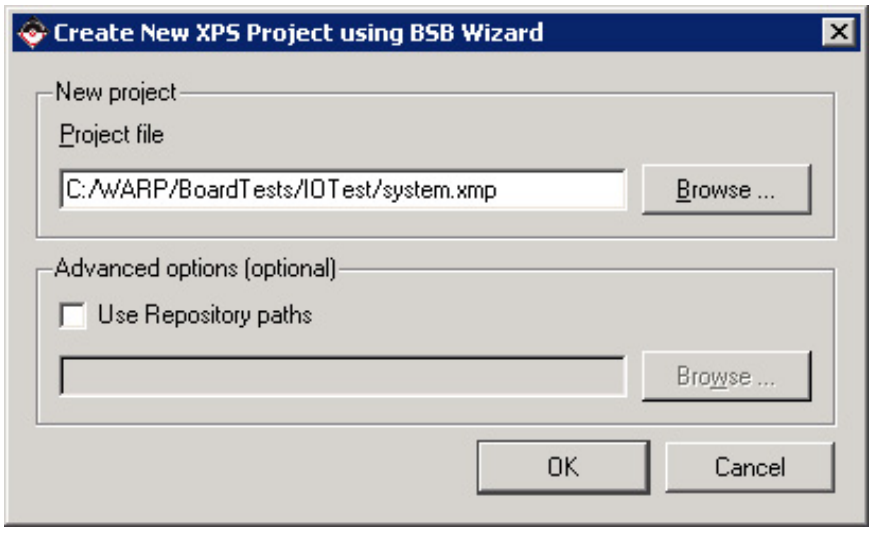

Figure 2: Step 3 – Choose a directory for *system.xmp*

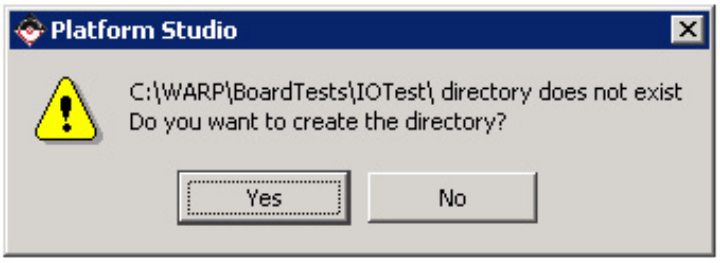

Figure 3: Step 3 – Click **Yes** to create the directory.

4. The **Base System Builder - Welcome** window should appear. Select **I would like to create a new design**, and click **Next**

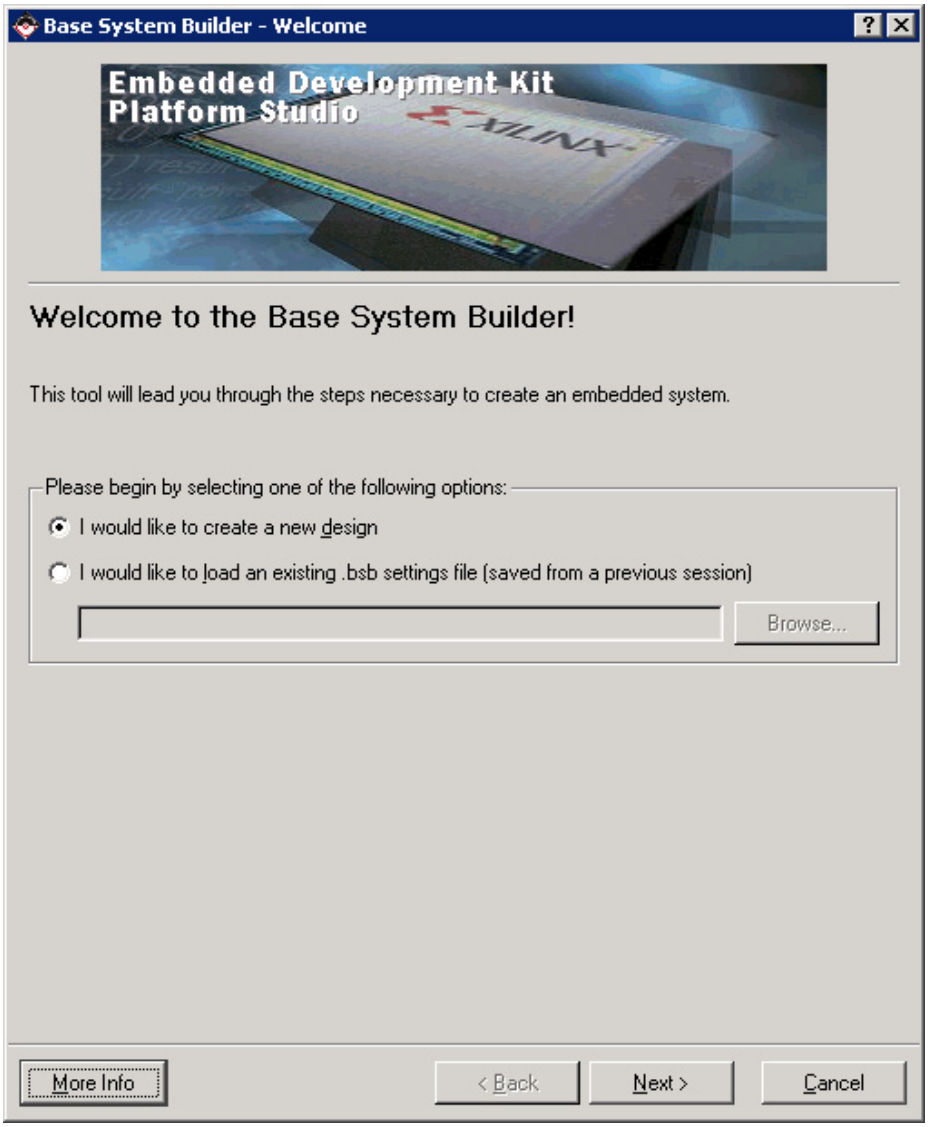

Figure 4: Step 4 – Welcome Screen

5. At the **Select Board** window, make the following selections and click **Next**:
   - Board vendor: *Rice University CMC - WARP Project*
   - Board name: *WARP FPGA and Radio Boards*
   - Board revision: *1.0b*

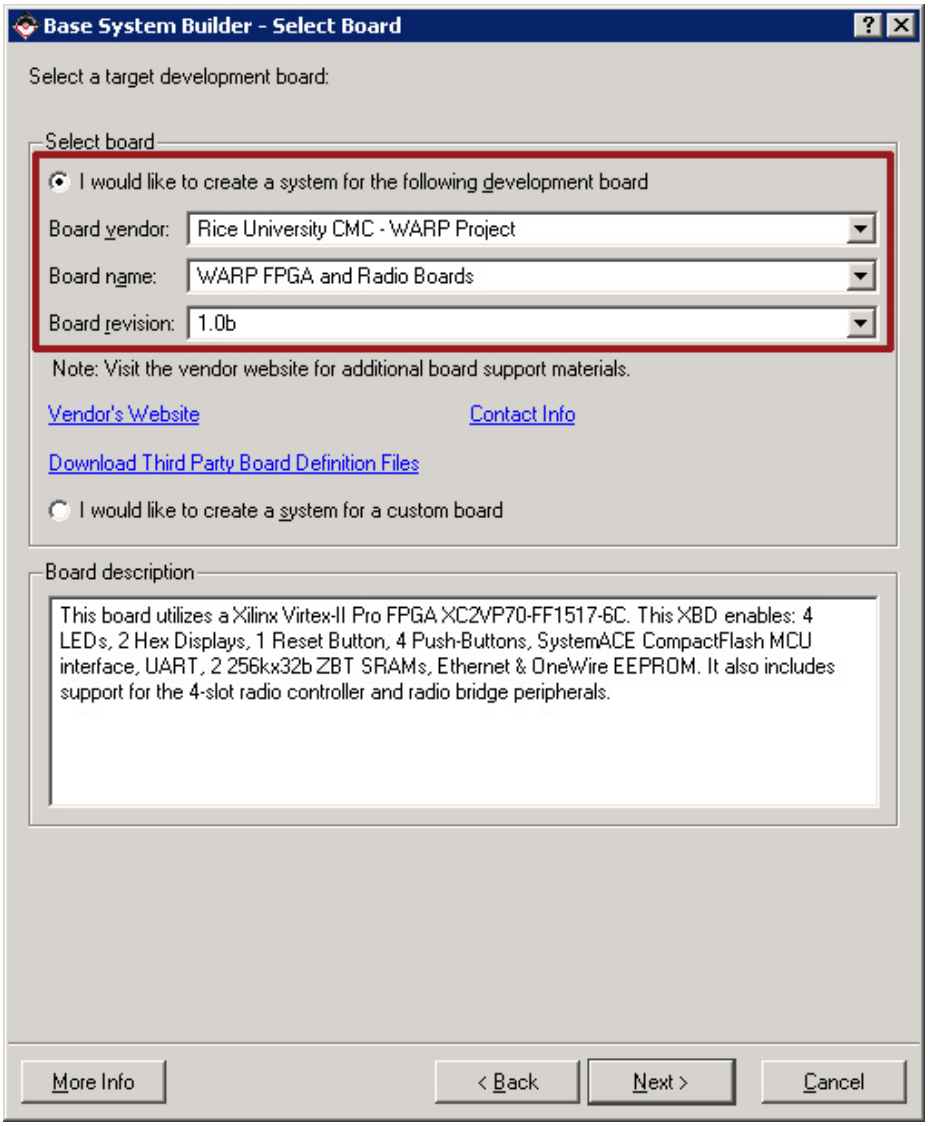

Figure 5: Step 5 – **Select Board** window

6. Make sure **PowerPC** is your selected processor. Click **Next**

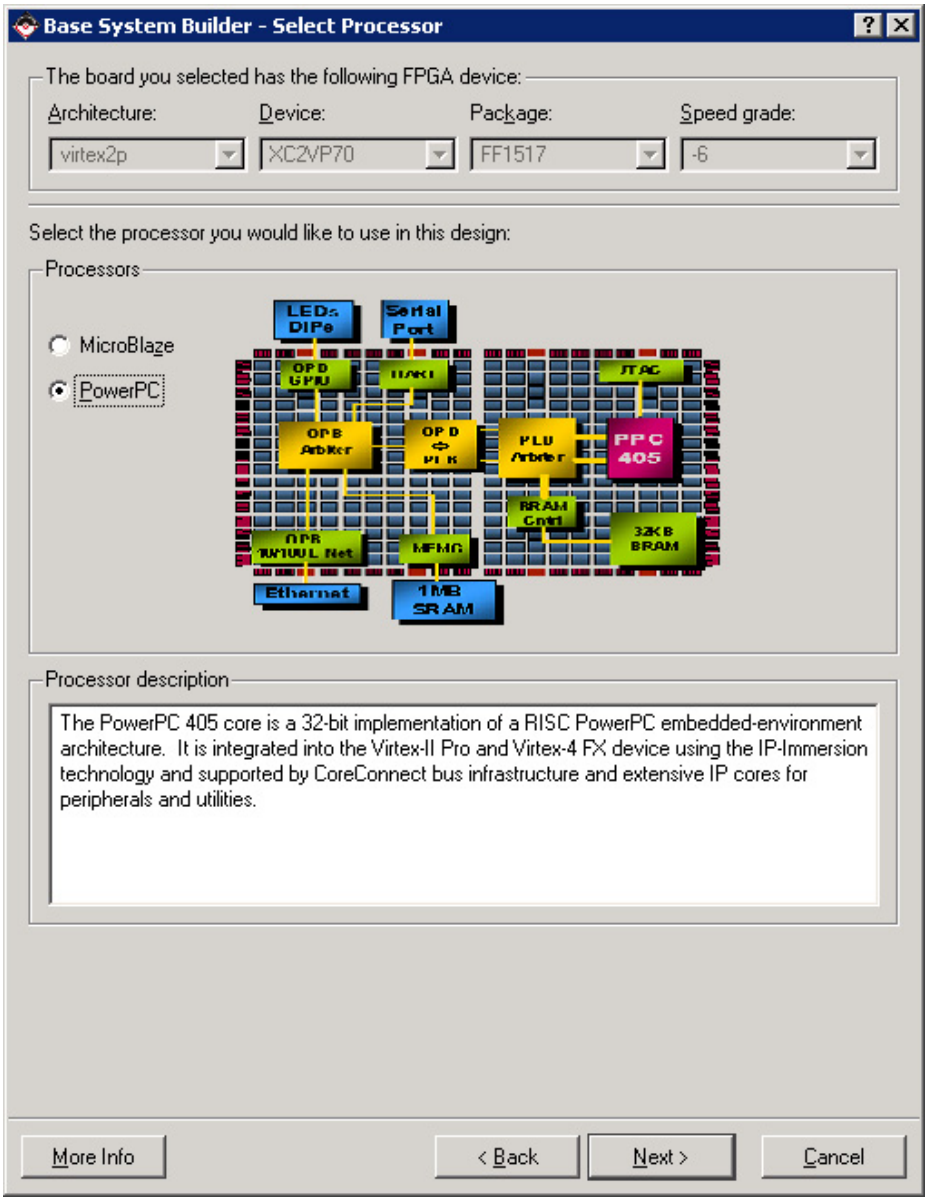

Figure 6: Step 6 – Processor Selection window

7. The **Configure PowerPC** window should appear, make the following designations and click **Next**:
   - Processor clock frequency: *100.00 MHz*
   - Bus clock frequency: *50.00 MHz*
   - Processor configuration: *FPGA JTAG*
   - On-chip memory (OCM)
     - Data: *64 KB*
     - Instruction: *128 KB*
   - Cache setup should be *unchecked*

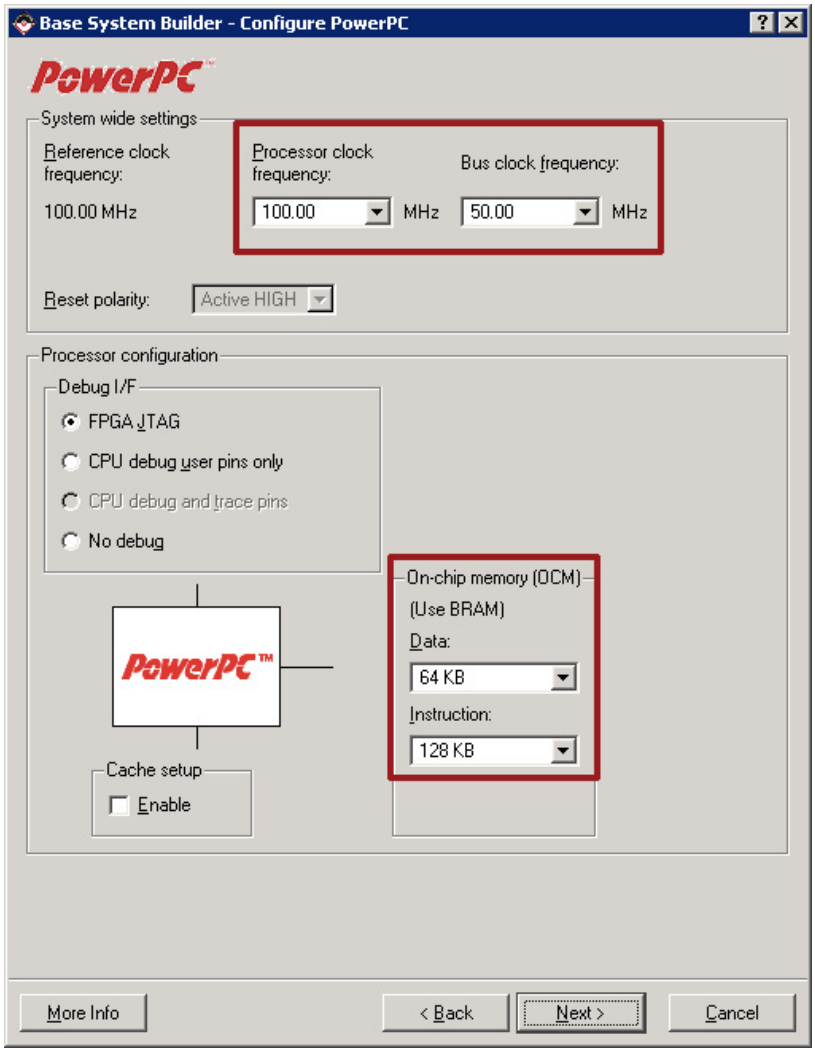

Figure 7: Step 7 – Configure PowerPC

8. The next windows are **Configure IO Interfaces**. Depending on the size of your window, a varying number of IO devices will be available on each screen. Make sure the following are checked (if an attribute is not enumerated, assume default configuration):
   - *LED_7SEGMENT*
   - *LED_7SEGMENT_1*
   - *LEDs_4Bit*
   - *Push_Buttons_4bit*
     - Check **Use interrupt** for the Push_buttons_4bit IO device.
       IMPORTANT: If you fail to do so now, consult the Help Documentation to learn how to add them once the project is created.
   - *RS232*
     - Peripheral: *OPB UARTLITE*
     - Baudrate: *57600*
   - *DIPSWs_4bit*
   - **UNCHECK**: *SysACECompactFlash*, *Ethernet_MAC*,*onewire_0*, *radio_controller_0*, *radio_bridge_slot_2*, *SRAM0_ZBT_512Kx32*, and *SRAM1_ZBT_512Kx32*

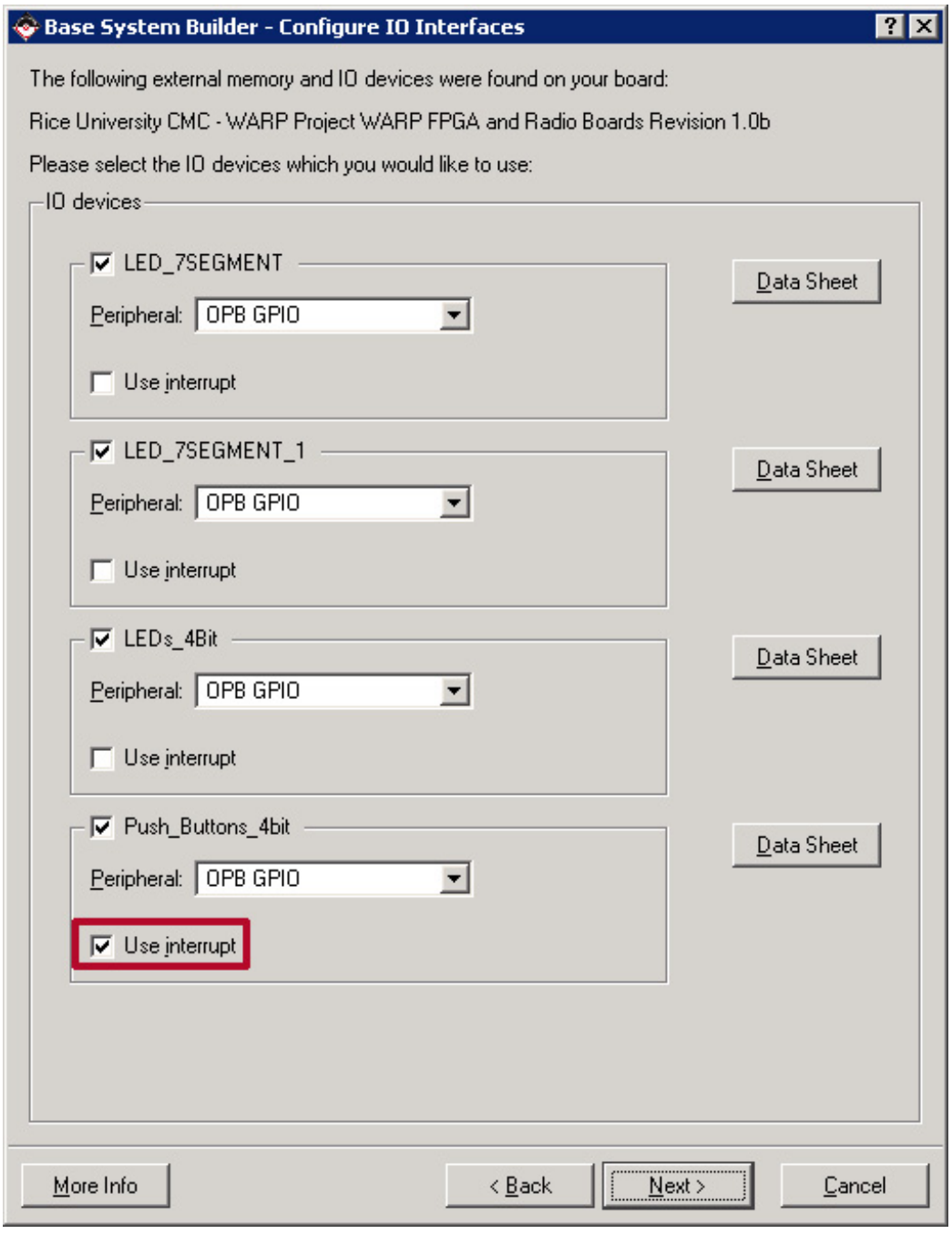

Figure 8: Step 8 – Choosing Peripherals

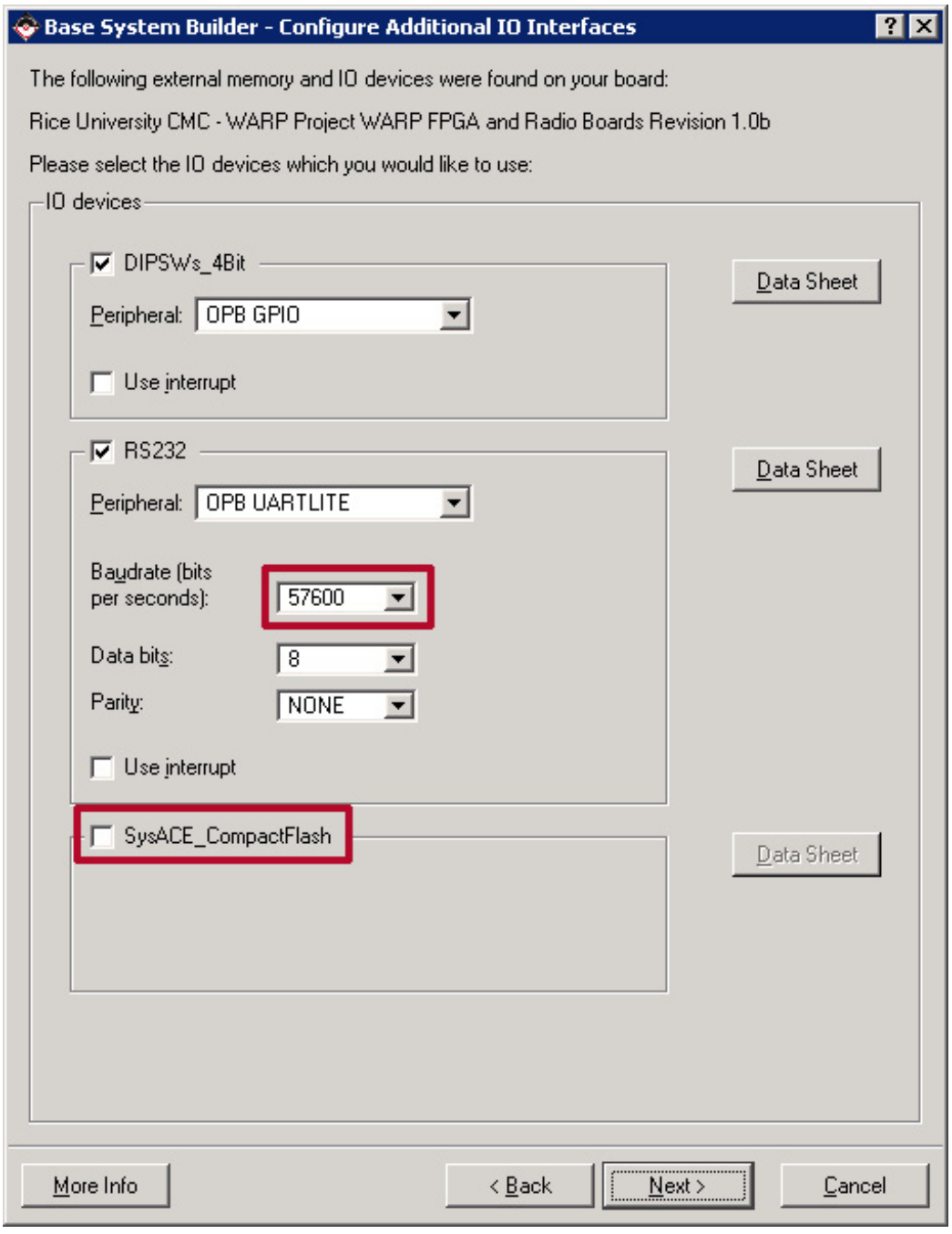

Figure 9: Step 8 – Choosing Peripherals cont.

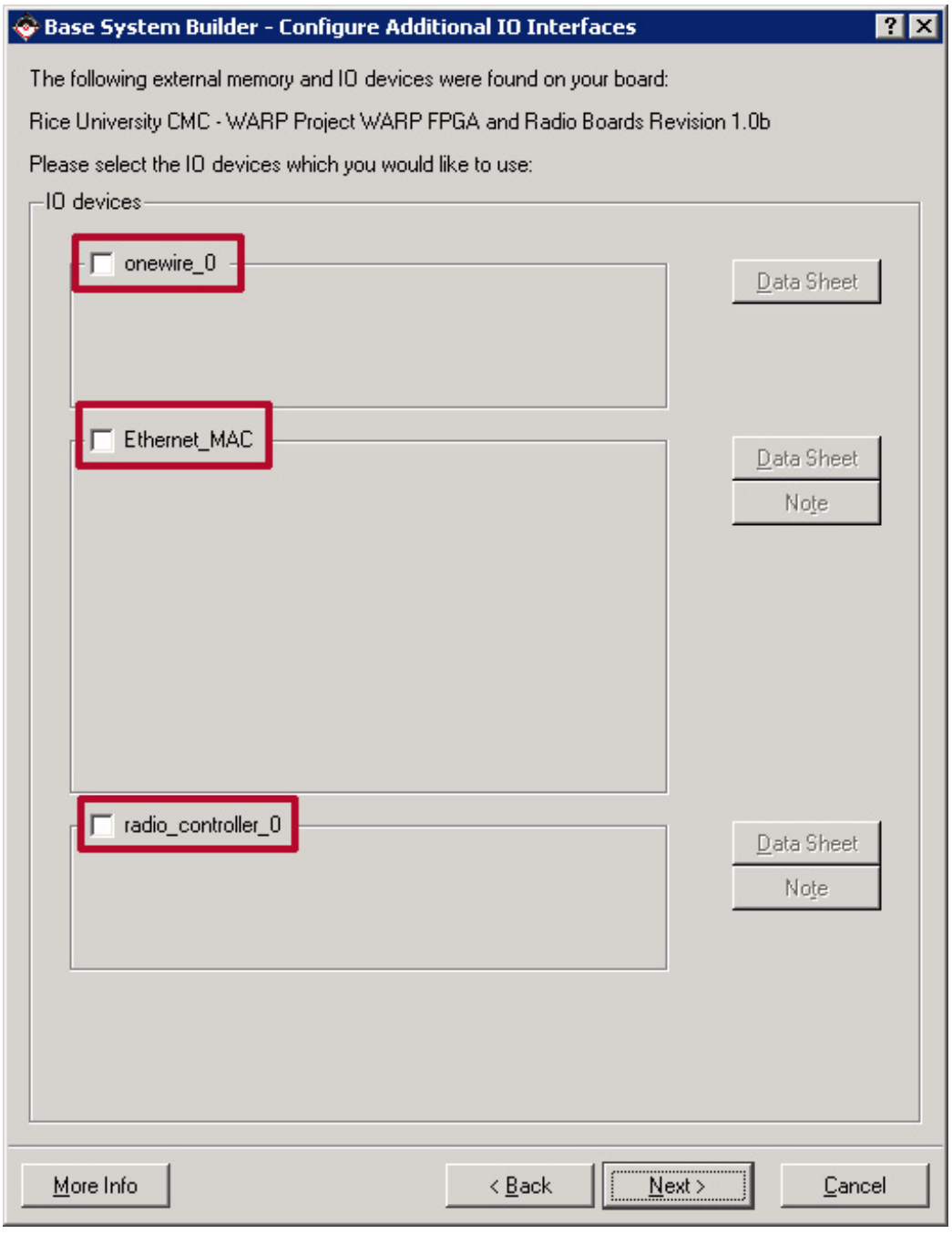

Figure 10: Step 8 – Choosing Peripherals cont.

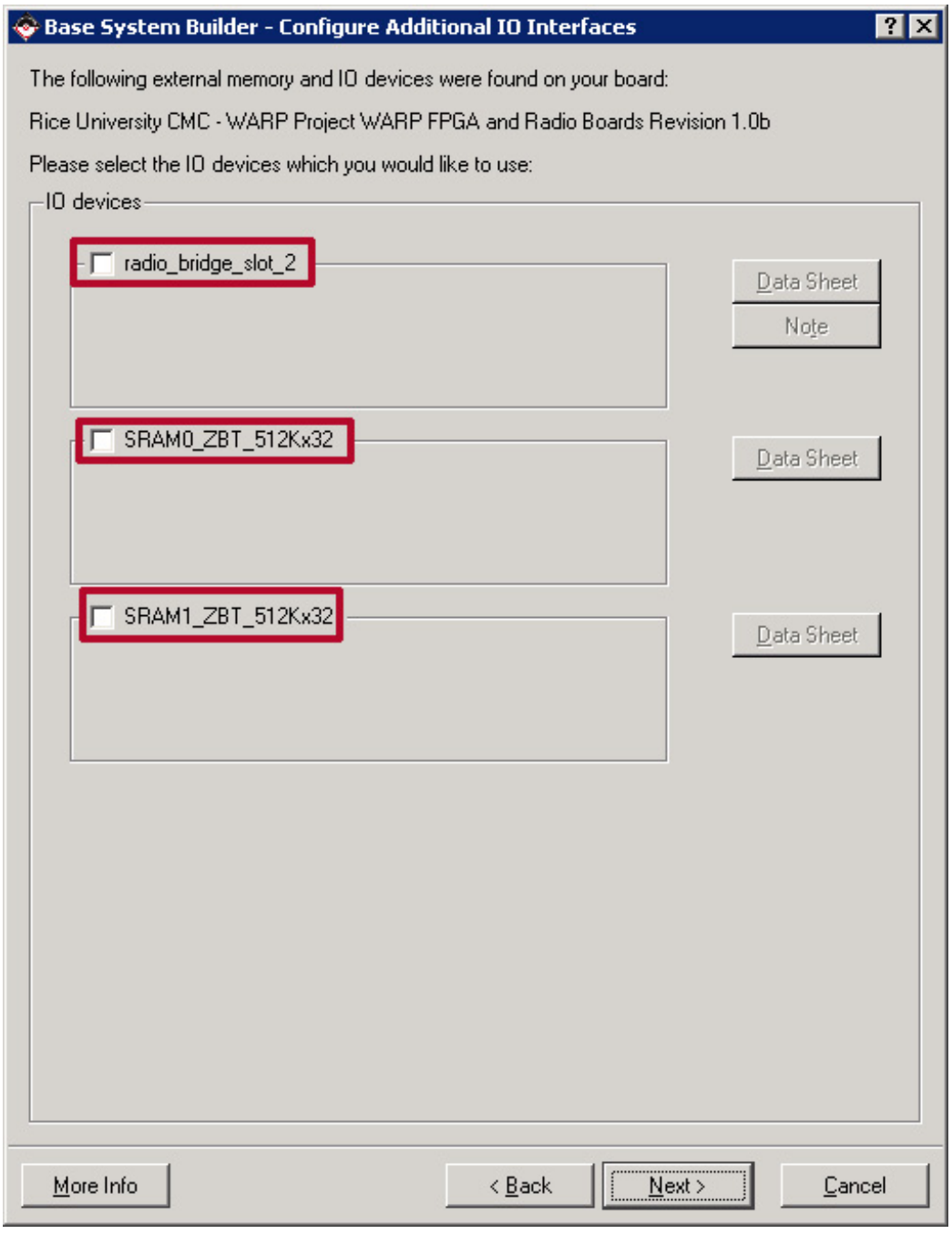

Figure 11: Step 8 – Choosing Peripherals cont.

9. At **Add Internal Peripherals**, click **Remove** to the right of the **plb_bram_if_cntlr_1 box**. Click **Next**

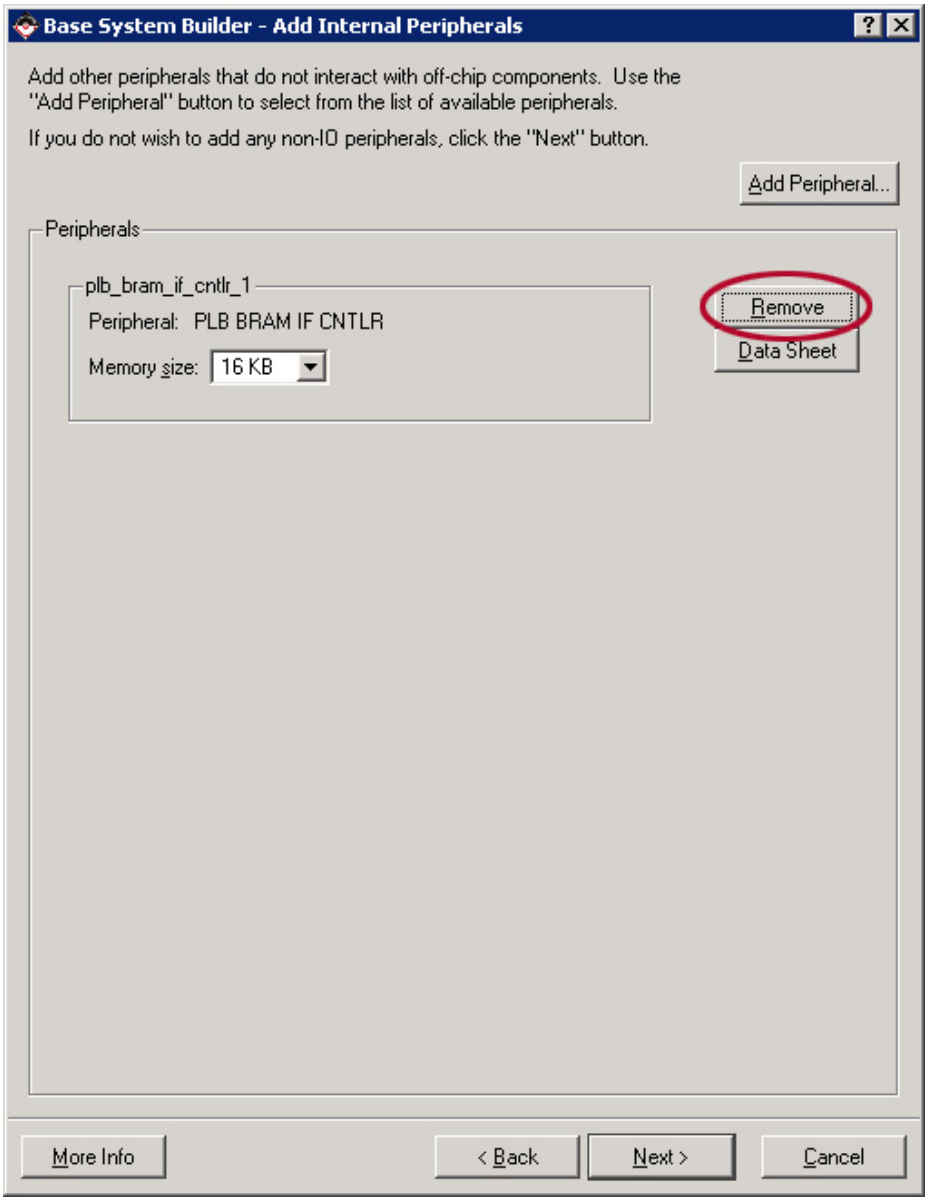

Figure 12: Step 9 – Before Removing

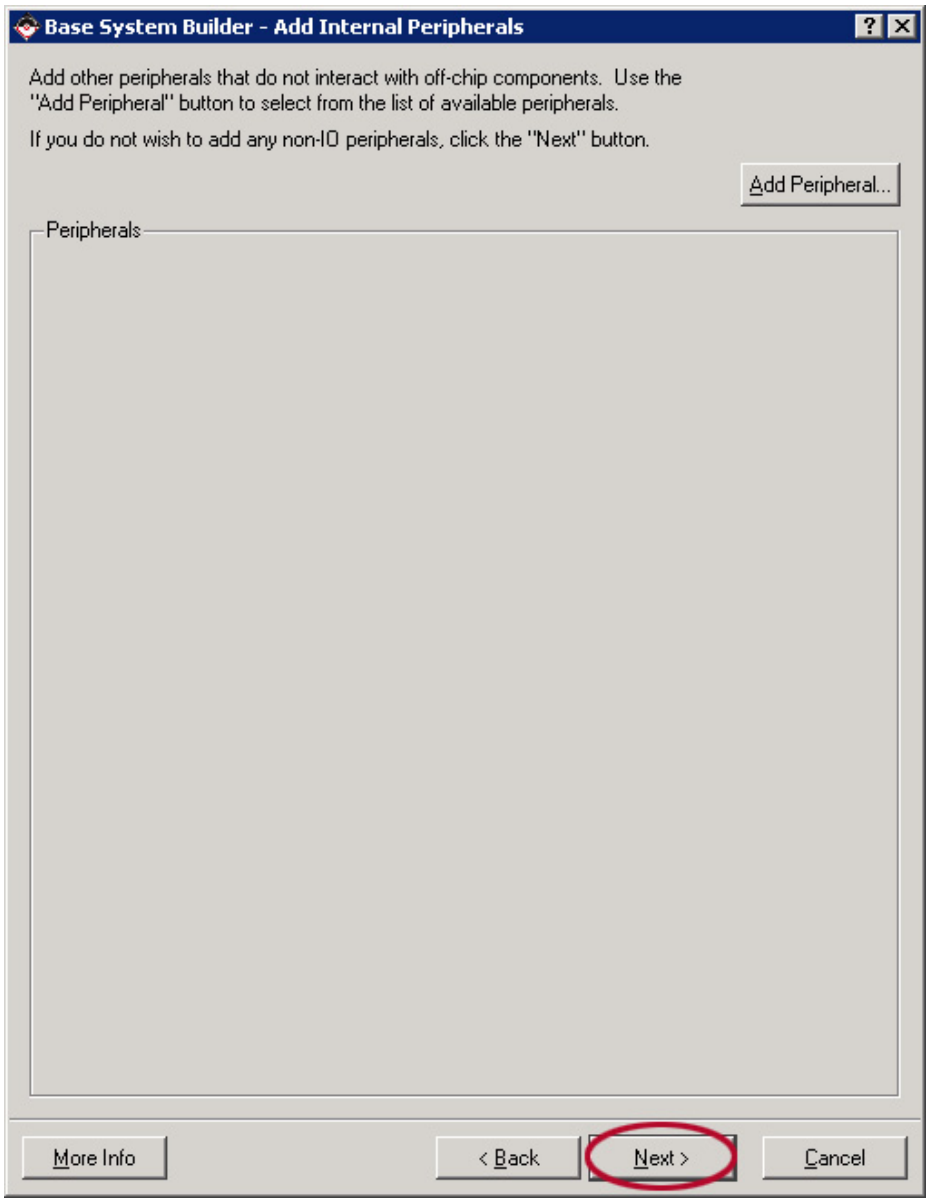

Figure 13: Step 9 – After Removing

10. At **Software Setup**, UNCHECK **Memory test** and **Peripheral selftest**. **RS232** should be chosen for **STDIN** and **STDOUT**. Click **Next**.

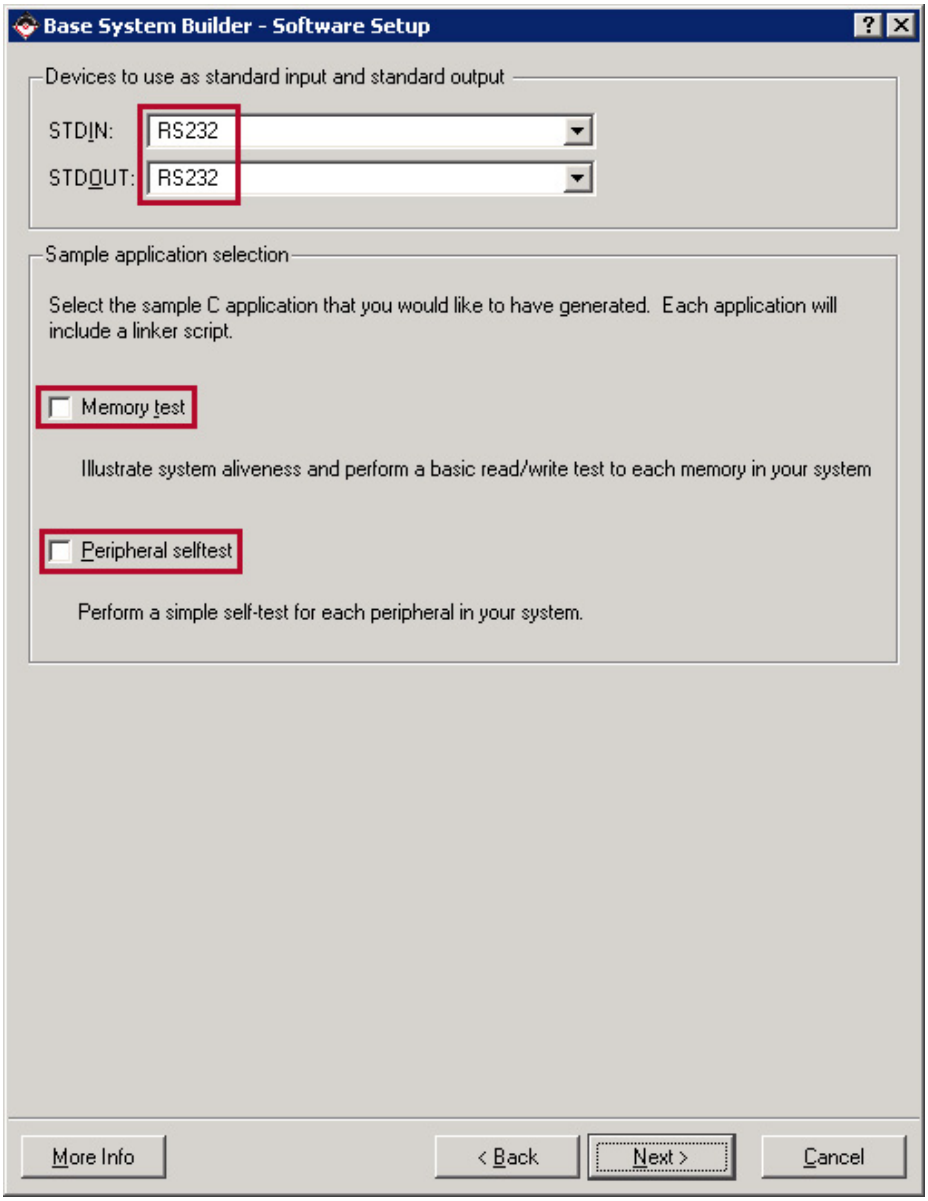

Figure 14: Step 10 – Software Setup

11. If you chose to keep the “Memory test” or “Peripheral selftest” simply click **NEXT** through configuration menu(s). Click **Generate** at the **System Created** window. Click **Finish** to exit the builder. Click **OK** to beging using XPS.

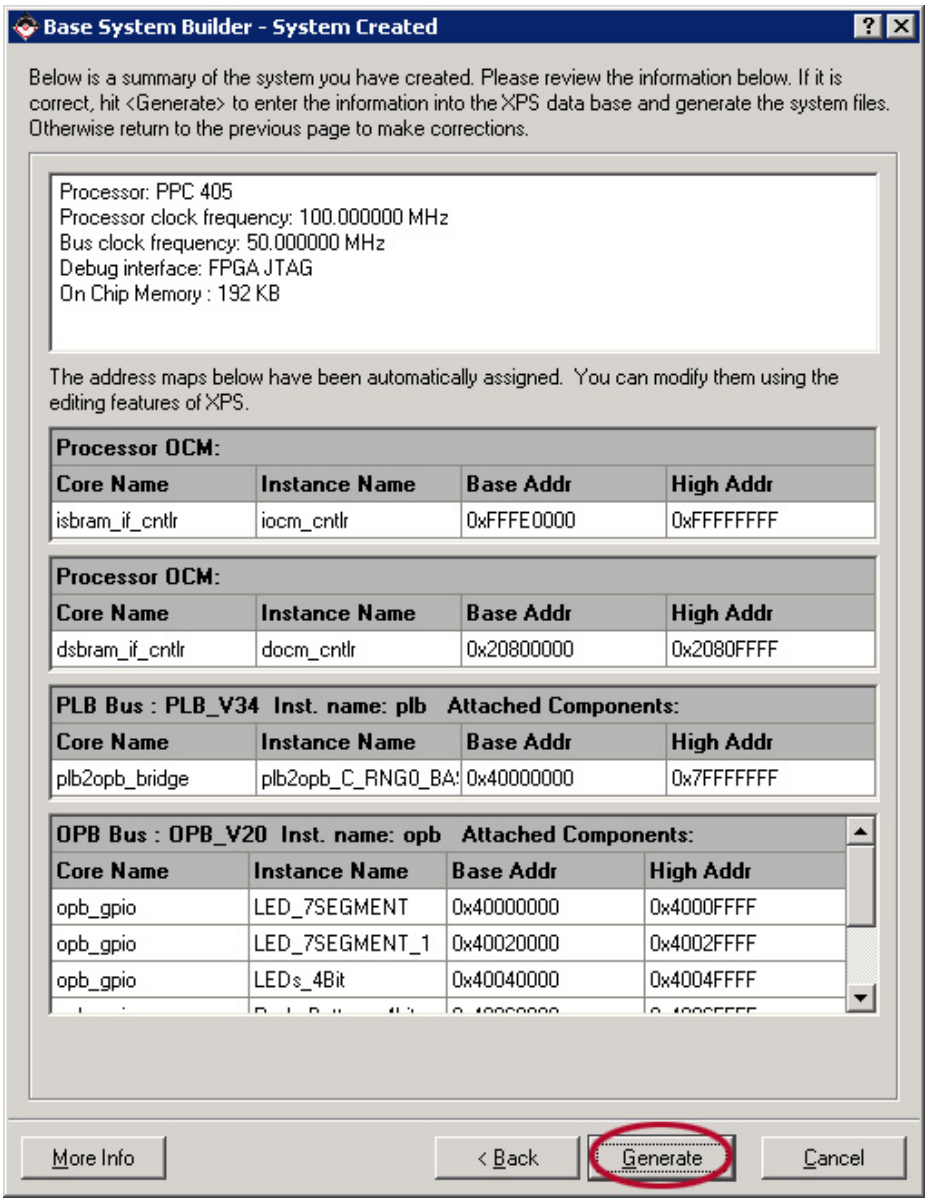

Figure 15: Step 11 – Generate File

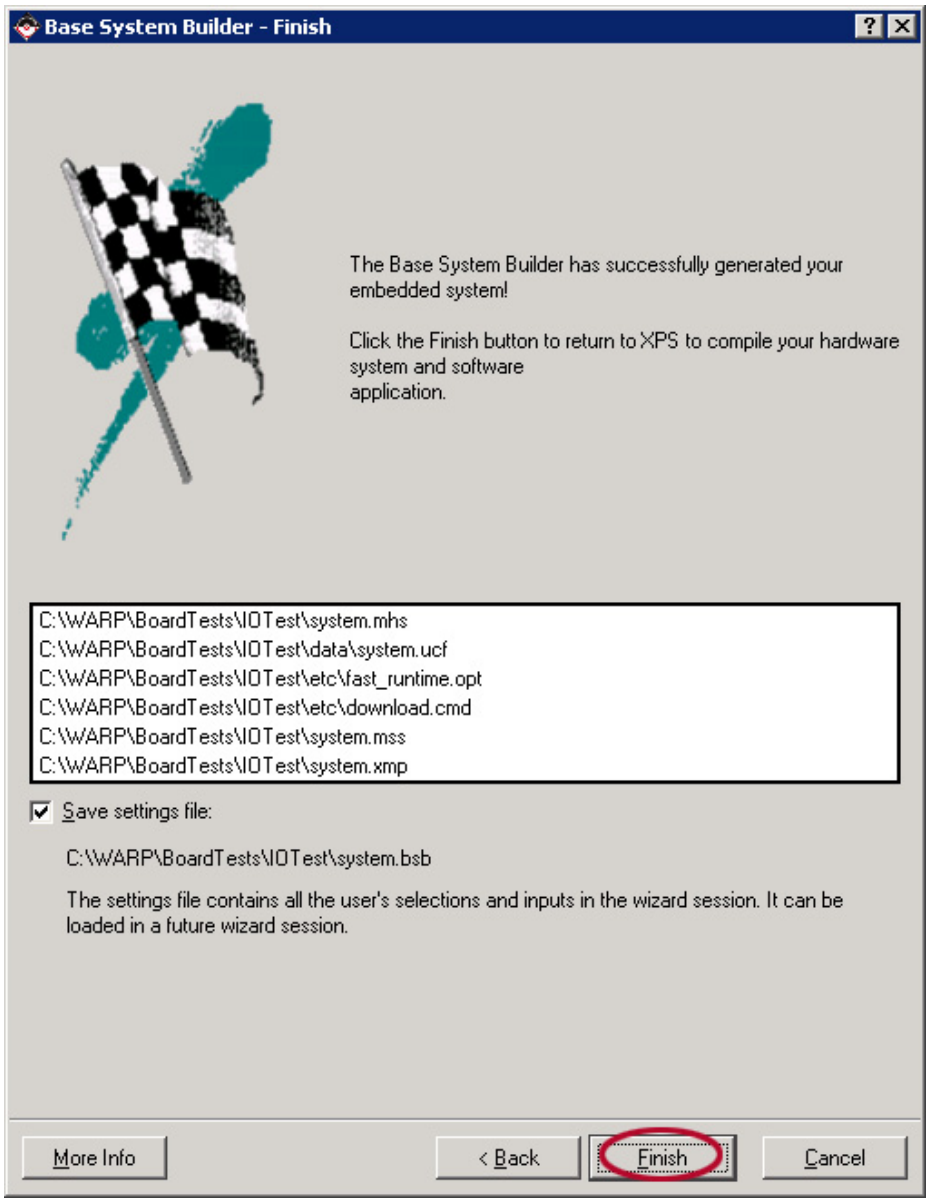

Figure 16: Step 11 – Finish

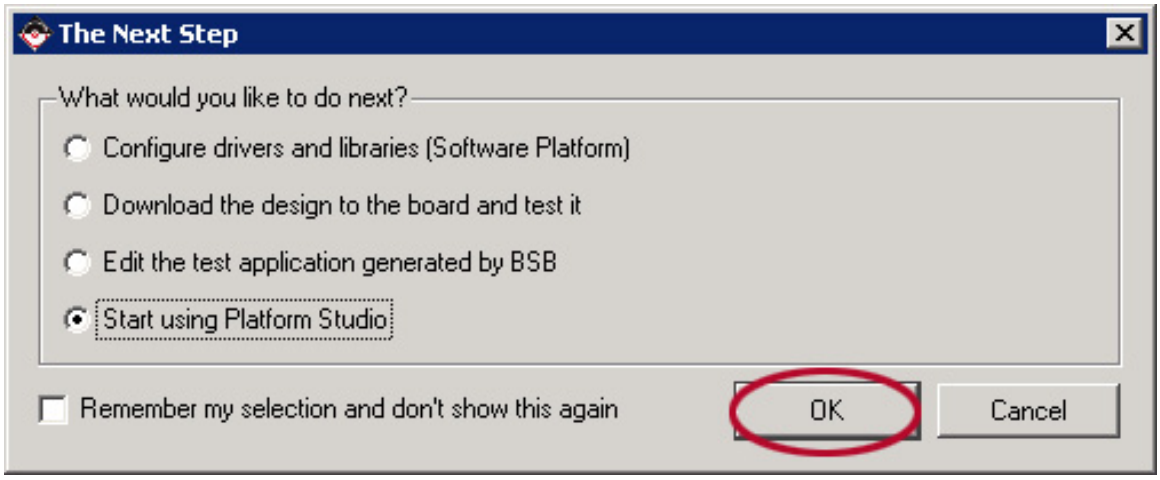

Figure 17: Step 11 – Start Working

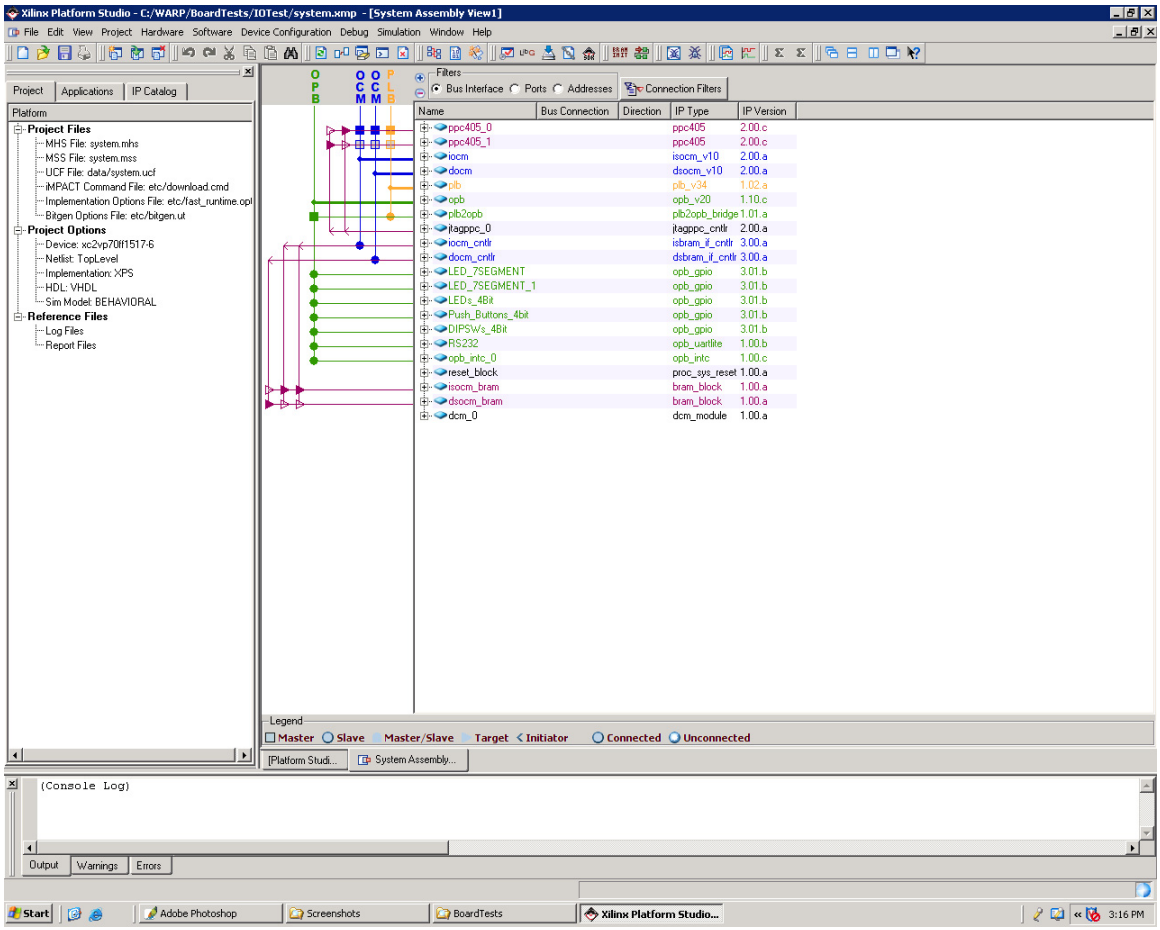

Figure 18: XPS Workspace after Base System Builder

2.2 Setting up the UserIO Test in XPS

1. Click on the **Applications** tab in the left hand box. Right-click on **Add Software Application Project...** and choose **Add Software Application Project...** Type in **UserIOTest**, and click **OK**. You should see you project in the list of "Software Projects".

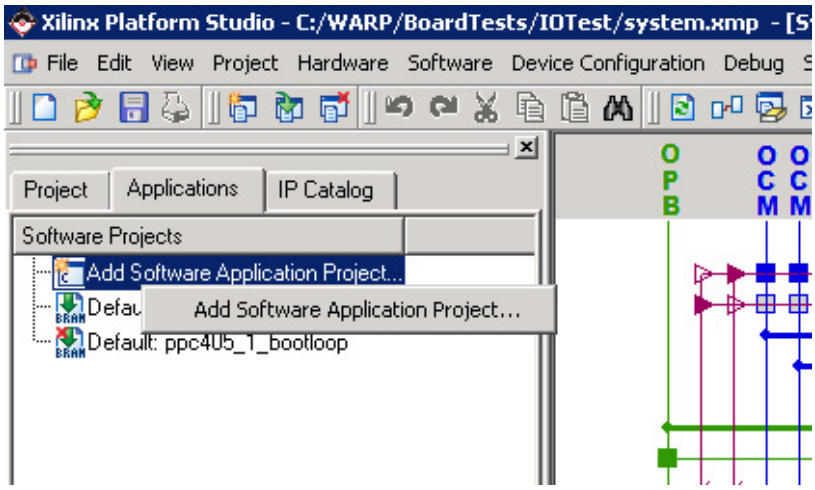

Figure 19: Step 1 – Adding a Software Project

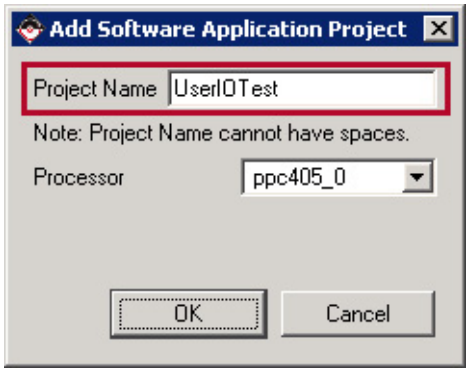

Figure 20: Step 1 – Name the project: UserIOTest

2. Right-click on **Sources** and choose **Add Existing Files...**
   Browse to **c:/WARP/BoardTests/Files**. You will want to add the following *.c files:
   - *warplib.c*
   - *UserIOTest.c*

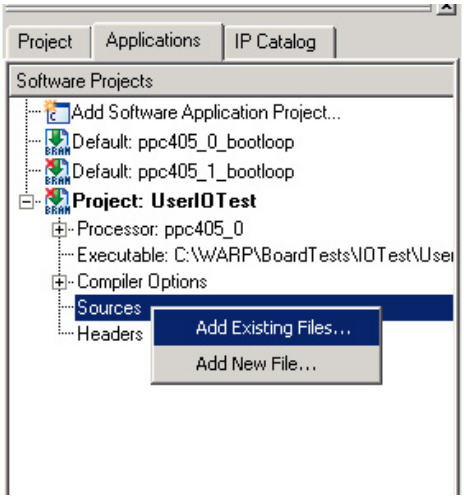

Figure 21: Step 2 – Adding Source Files

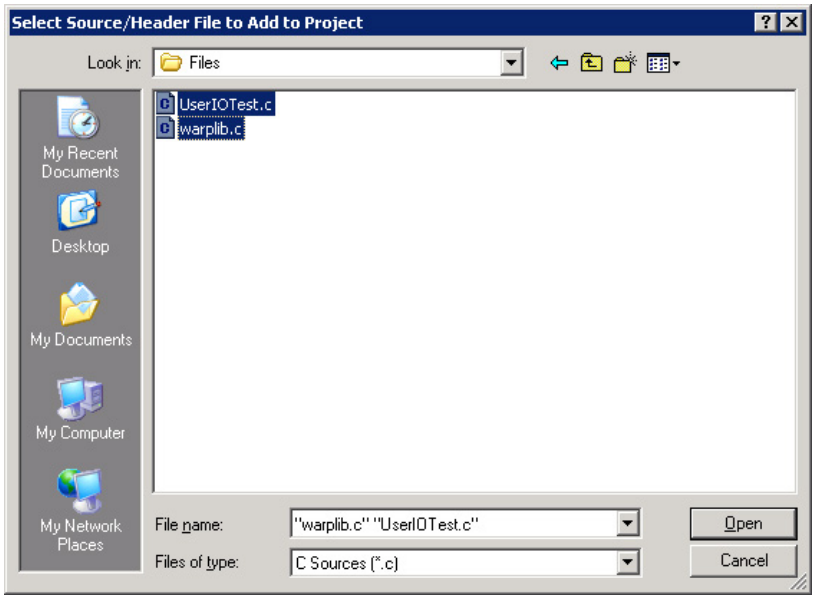

Figure 22: Step 2 – Select: UserIOTest.c and warplib.c

3. Next, right-click on **Headers** and choose **Add Existing Files...** You should already be in the correct folder.
   If you do not see *warplib.h*, browse to **c:/WARP/BoardTests/Files**. You will want to add the following *.h file:

   - *warplib.h*

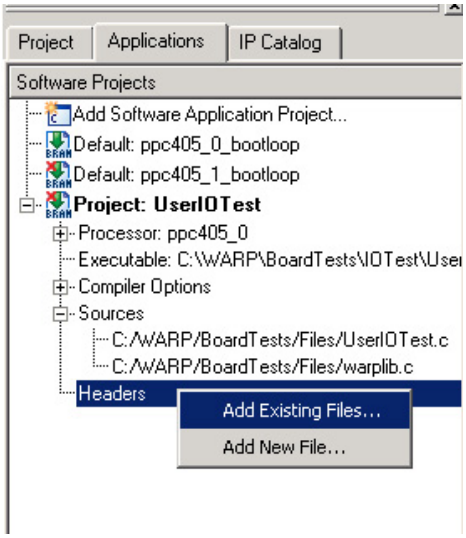

Figure 23: Step 3 – Adding Header Files

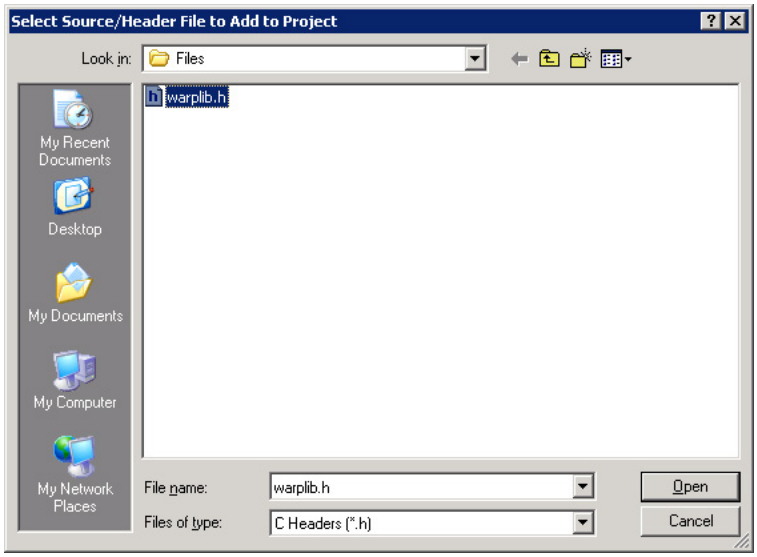

Figure 24: Step 3 – Select: warplib.h

4. Right-click on **Default: ppc405_0_bootloop** in the right hand menu. Uncheck **Mark to Initialize BRAMs**. Afterward, there should be a red 'x' over the green arrow next to the name.

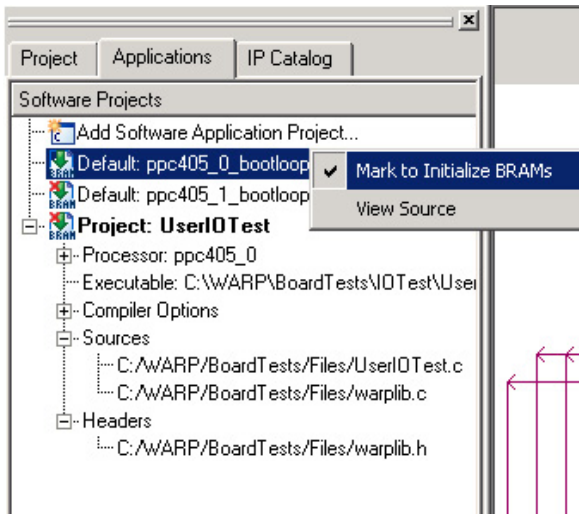

Figure 25: Step 4 – Uninitializing BRAMs for the Default

5. Right-click on **Project: UserIOTest** and check **Mark to Initialize BRAMs**. This step tells XPS to update the bitstream with your project. Afterward, there should no longer be a red 'x' over the green arrow next to the name.

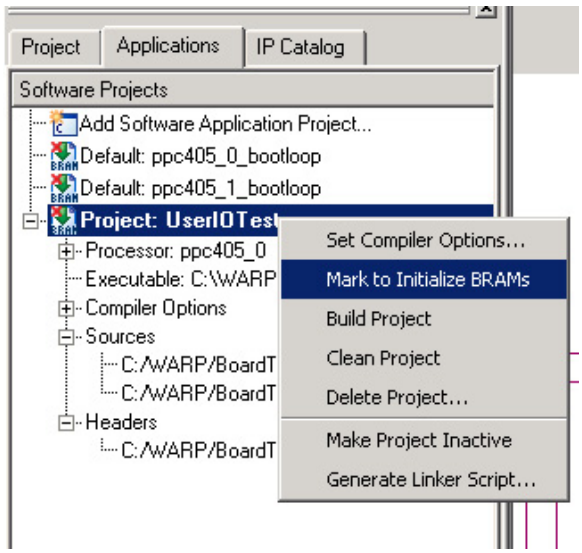

Figure 26: Step 5 – Initializing BRAMs for UserIOTest

6. Right-click on **Project: UserIOTest** and select **Generate Linker Script**. Make sure that each article under the **Memory** drop down menus is either set to **iocm_cntlr** or **docm_cntlr**. Click **Generate**

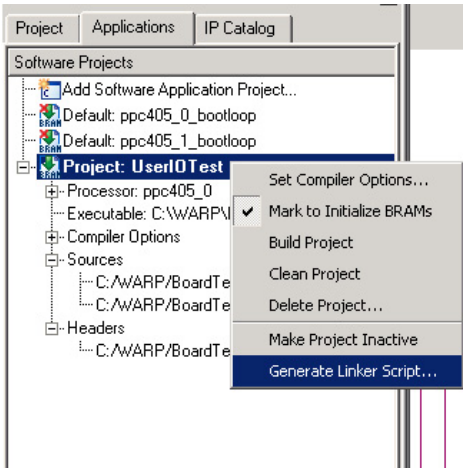

Figure 27: Step 6 – Generate Linker Script

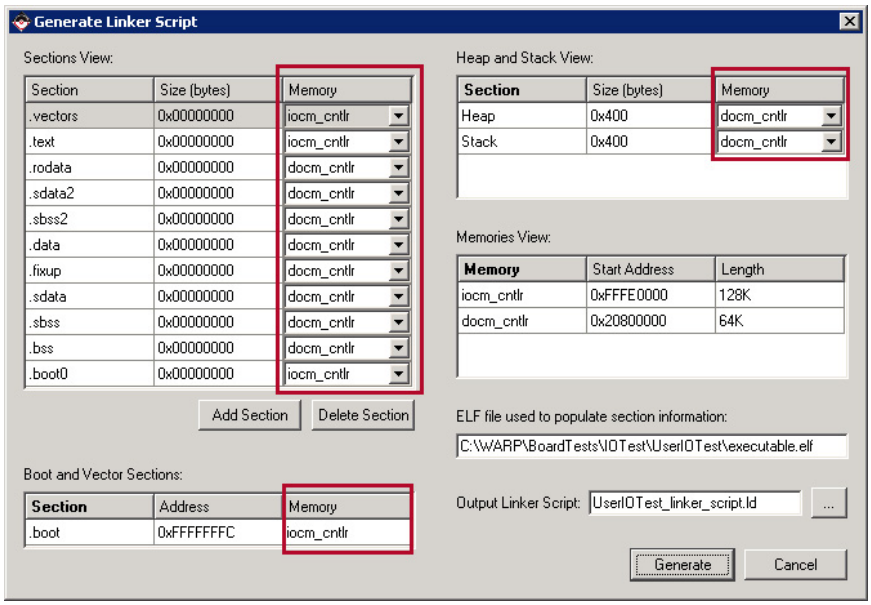

Figure 28: Step 6 – Set memory to iocm_cntlr or docm_cntlr

7. Choose **Update Bitstream** by either accessing it through **Device Configuration** on the top menu, or by clicking on the toolbar button (it says “Bram Init” on it). This process will take 10-15 minutes depending on your computing speed. Longer may indicate an improper setup (esp. steps 4,5,6 of this section).

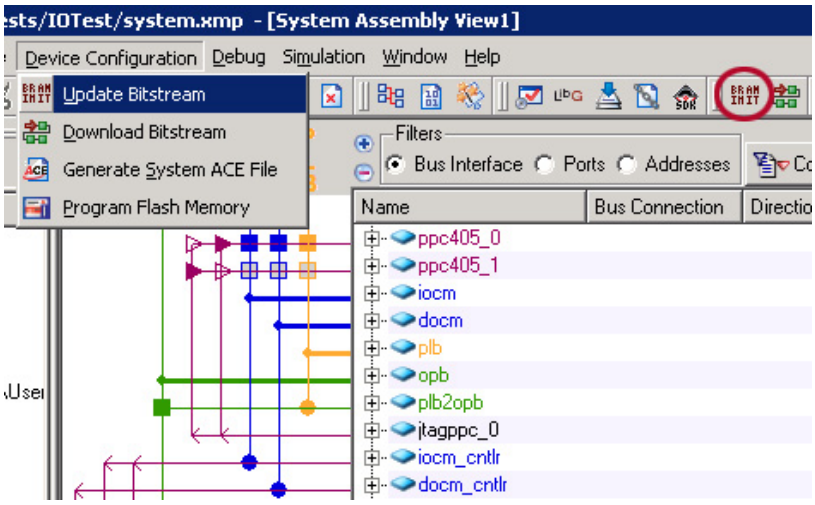

Figure 29: Step 7 – Update Bitstream

8. The file is now ready to download to the board.

For help, please refer to the Help/FAQ page.

3 Running the Program

3.1 Ready Tera Term Pro

1. Open Tera Term Pro (Browse to "**Program Files****TTERMPRO****ttermpro.exe**")
2. Choose **Serial** and select the appropriate COM port (the one to which the board is connected) from the **Port**: drop down menu.

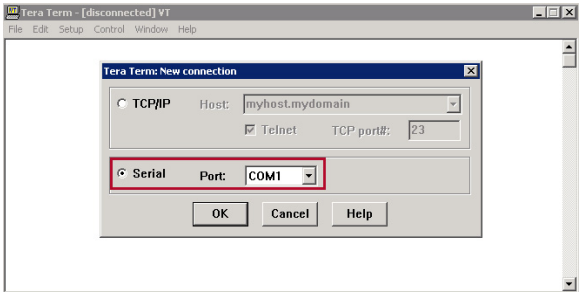

Figure 30: Step 2 – Tera Term Opening Dialog

3. Go to **Setup** → **Serial Port...** and change the **Baud rate** to **57600** (or whatever you specified in your project) from the drop down menu. Click **OK**

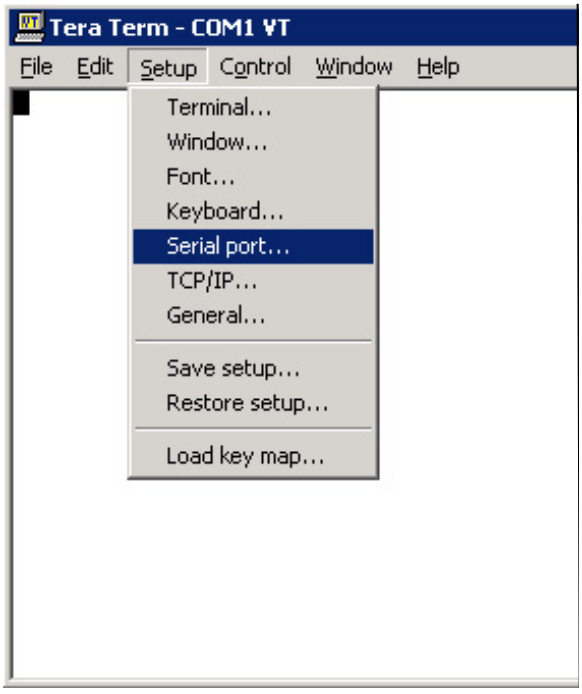

Figure 31: Step 3 – Change Serial Port Settings

4. Tera Term is now ready to receive data.

NOTE: (If you are unsure about what rate you choose, this can be found by double-clicking **RS232** in the **System Assembly** view. It is the number given for **UART Lite Baud Rate**).

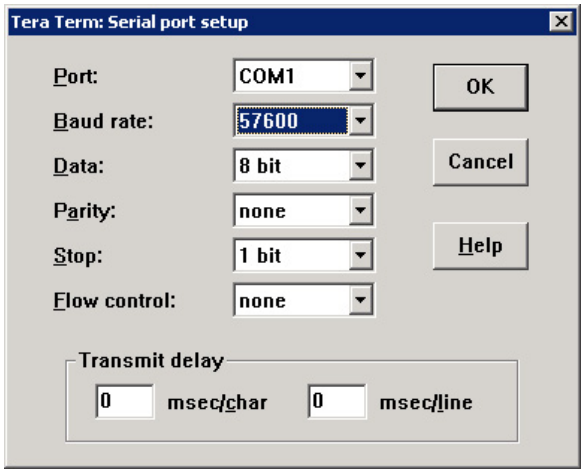

Figure 32: Step 3 – Serial Port Settings

3.2 Download Peripheral Test to the Board

(Assumes that the board has been connected and powered and that the bitstream has been generated successfully)

3.2.1 Method 1: Directly from XPS

1. Download the bitstream to the board via **Device Configuration** → **Download Bitstream** or by clicking on the toolbar icon. (NOTE: XPS will recompile/regenerate everything that is not current before downloading the bitstream)

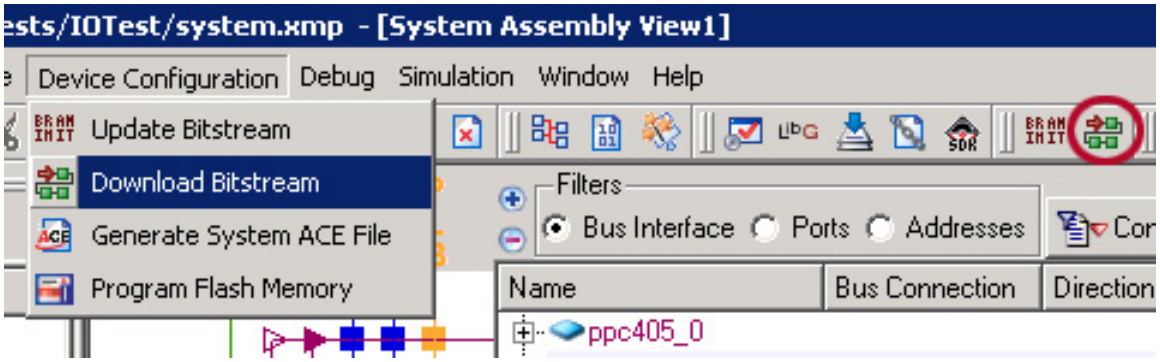

Figure 33: Step 1 – Download Bitstream

3.2.2 Method 2: Using iMPACT

1. Open iMPACT via **Program Files** → **Xilinx ISE 8.1i** → **Accessories** → **iMPACT**
2. When the **iMPACT Project** dialogue box pops up, click **Cancel** You should see the workspace.
3. Right-click on the workspace and choose **Initialize Chain**. Click **OK** at the **Boundary-Scan Chain Contents Summary** window.
4. You will see the **Assign New Configuration File** window. Click **Bypass** for the **xccace** (first) block.

5. For the **xc2vp70** block, browse to the location of your generated bitstream (e.g. "\ProjectFolder\implement Select this file and click **Open**. Click **OK** at the **Add Virtex-II Pro/Virtex-4 Object Files** window to return to the workspace.
6. Right click on the **xc2vp70** block, and choose **Program**. Click **OK** to download to the board.

3.2.3 Method 3: Using ChipScope

1. Open ChipScope via **Program Files** → **ChipScope Pro 8.1i** → **ChipScope Pro Analyzer**
2. Click on the **Open Cable/Search JTAG Chain** button located in the upperleft corner.
3. Click **OK** at the window that pops up.
4. Right click on **xc2vp70** in the box in the upper-lefthand corner. Choose **Configure**.
5. Choose **Select New File** and browse to the location of your generated bitstream (e.g. "\ProjectFolder\impl
6. Click OK to download to the board.

4 FAQ

4.1 QUESTIONS

1. **I forgot to enable interrupts for the push buttons when using Base System Builder. What do I do now?**
2. **What do I do if I didn't select one of the devices while using Base System Builder?**
3. **I get an error: "*** No rule to make target 'File name', needed by 'UserIOTest/executable.elf'. Stop"**
4. **Where can I get Tera Term Pro?**
5. **When I download my project (download.bit) to the board, nothing happens.**
6. **My project takes a longtime to generate the bitstream. Then it doesn't work. What's wrong?**
7. **Everything looks right, but when I try downloading to the board with iMPACT, nothing happens.**
8. **I get an error: "built in linker script:[line#] cannot move location counter backwards (from [address1] to [address2])"**
9. **When all else fails...**

4.2 ANSWERS

1. **I forgot to enable interrupts for the push buttons when using Base System Builder. What do I do now?**
   - Copy the following lines of code into the MHS file:

     ```
     BEGIN opb_intc
     PARAMETER INSTANCE = opb_intc_0
     PARAMETER HW_VER = 1.00.c
     PARAMETER C_BASEADDR = 0x41200000
     PARAMETER C_HIGHADDR = 0x4120ffff
     BUS_INTERFACE SOPB = opb_newline
     PORT Intr = Push_Buttons_4bit_IP2INTC_Irpt
     PORT Irq = EICC405EXTINPUTIRQ
     END
     ```

   - Add these lines to the Push_Buttons_4bit instance in the MHS file (the first parameter in each device in the instance name):

     ```
     PARAMETER C_INTERRUPT_PRESENT = 1
     PORT IP2INTC_Irpt = Push_Buttons_4bit_IP2INTC_Irpt
     ```

   - Add this line to the ppc405_0 instance in the MHS file:

     ```
     PORT EICC405EXTINPUTIRQ = EICC405EXTINPUTIRQ
     ```

   - Add these lines to the MSS file:

     ```
     BEGIN DRIVER
     PARAMETER DRIVER_NAME = intc
     PARAMETER DRIVER_VER = 1.00.c
     PARAMETER HW_INSTANCE = opb_intc_0
     END
     ```

If this does not work, you will need to recreate the project using Base System Builder

2. **What do I do if I didn't select one of the devices while using Base System Builder?**
   - For the size of this project, it will be easier to simply recreate the project using Base System Builder. You can clear out the contents of the directory containing all the current files, or simply create a new folder in which to store the new project.
3. **I get an error: "*** No rule to make target 'File name', needed by 'UserIOTest/executable.elf'. Stop"**
   - Check to see that there are no spaces anywhere in the names of your source and header paths. XPS will give the above error if there are.
4. **Where can I get Tera Term Pro?**
   - http://www.vector.co.jp/authors/VA002416/teraterm.html
5. **When I download my project (*download.bit*) to the board, nothing happens.**
   - Did the lowest LED light up up downloading?
     - Yes? This indicates that the program has reached the board but that there may be something wrong with the serial connection. Check these and try again.
     - No? This indicates that the program never got to your board. Check the JTAG connection and try again. Then move to the following questions.
   - Do the baud rates match between your project and Tera Term?
     - See Step 3 and "NOTE" on the **Running the Program** page
   - Review Steps 2-6 of **Setting up the UserIO Test in XPS**
6. **My project takes a longtime to generate the bitstream. Then it doesn't work. What's wrong?**
   - Refer to steps 4-6 of **Setting up the UserIO Test in XPS**
7. **Everything looks right, but when I try downloading to the board with iMPACT, nothing happens.**
   - Try restarting TeraTerm and iMPACT. If this doesn't work, try the other methods listed in the **Download Peripheral Test to the Board** section
8. **I get an error: "built in linker script:[line#] cannot move location counter backwards (from [address1] to [address2])"**
   - You need to regenerate the linker script because of changes to your code. Repeat step 6 of **Setting up the UserIO Test in XPS**: here. Click OK at the request to overwrite the previous script.
9. **When all else fails...**
   - Consult the help documentation provided by Xilinx accessible through the help menu (**Help** → **EDK Online Documentation** → Click **DOCUMENTS** tab). You may find the following most helpful:
     - Platform Specification Format
     - OS and Libraries Reference Guide
     - Processor IP Catalog