


WARP Analog Board

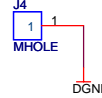
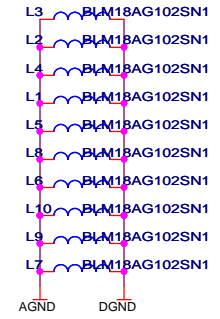
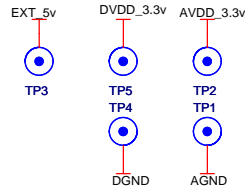
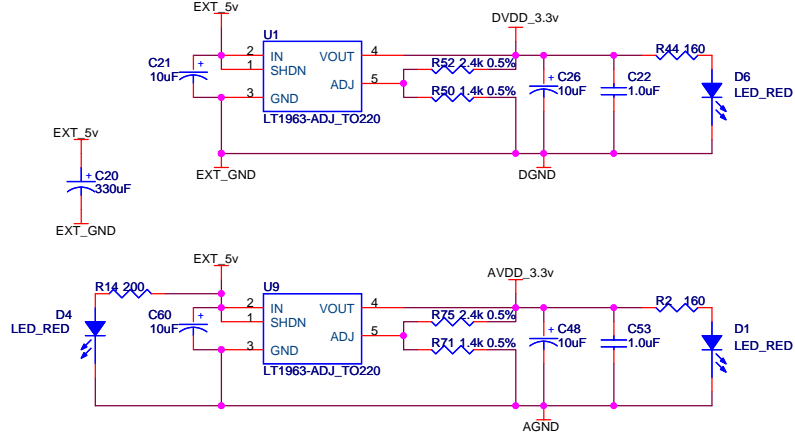
Revision 1.1

Schematic Pages

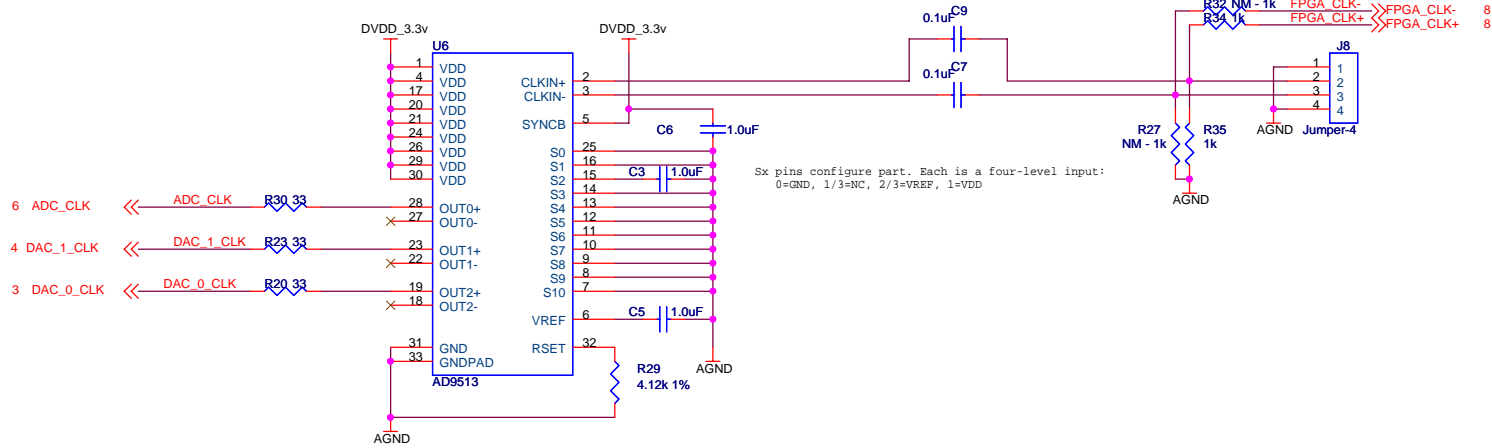
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5. D/A Converter Output Circuits
6. A/D Converter
7. A/D Converter Input Circuits
8. Daughter Card I/O
9. GrandDaughter Card I/O and Misc.

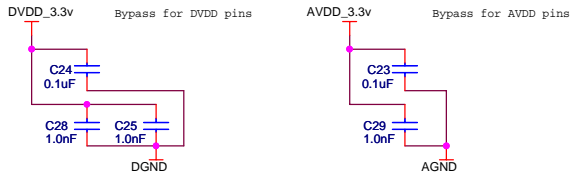
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|---|---------|---|
| Center for Multimedia Communication Rice University | |  |
| Title ADC/DAC Daughtercard | | |
| Description Daughtercard for WARP Platform for Data Conversion | | Rev 1.1 |
| Date: Wednesday, September 13, 2006 | Sheet 1 | of 9 |

Analog/Digital Ground Filtering

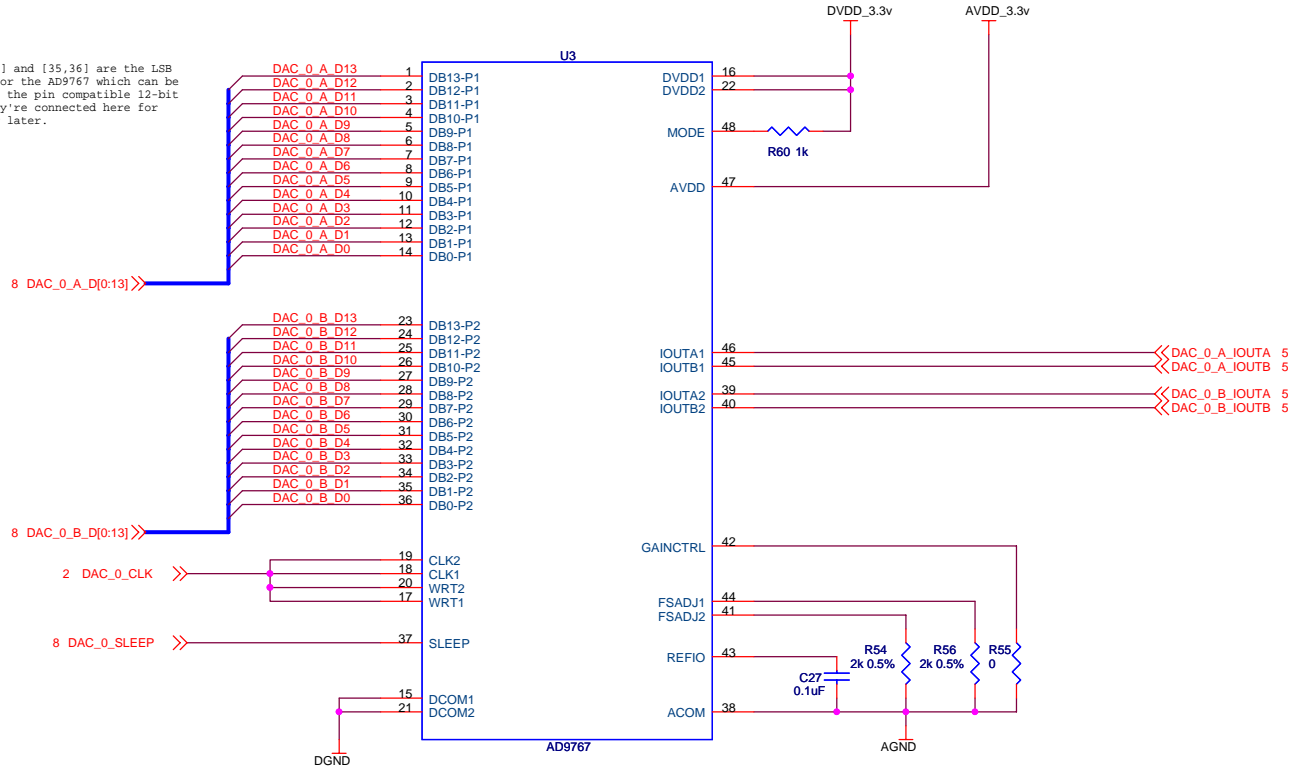


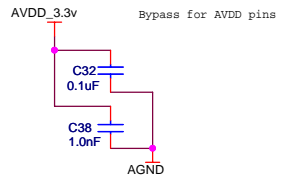
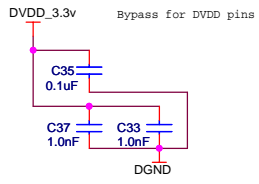
Mount these resistors to allow the FPGA to drive the clock input for the data converters. These *must* be removed to use the external clock connector.



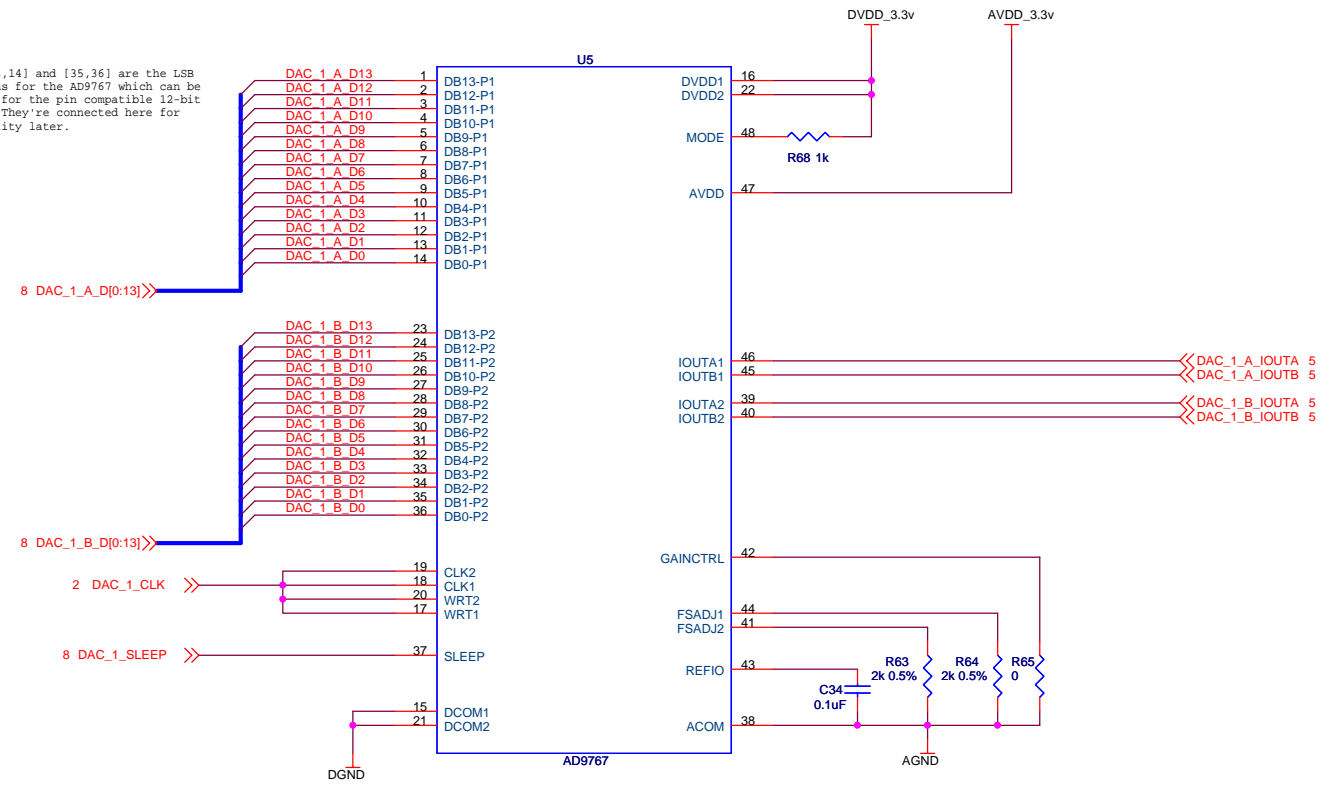


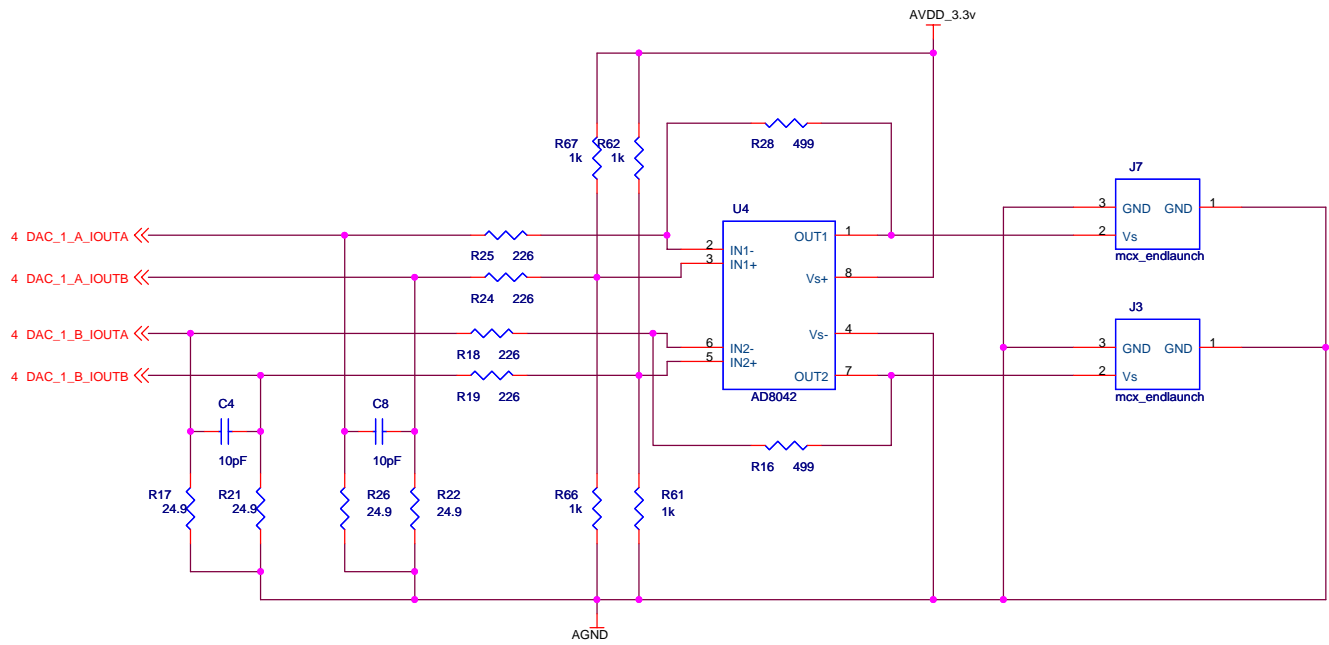
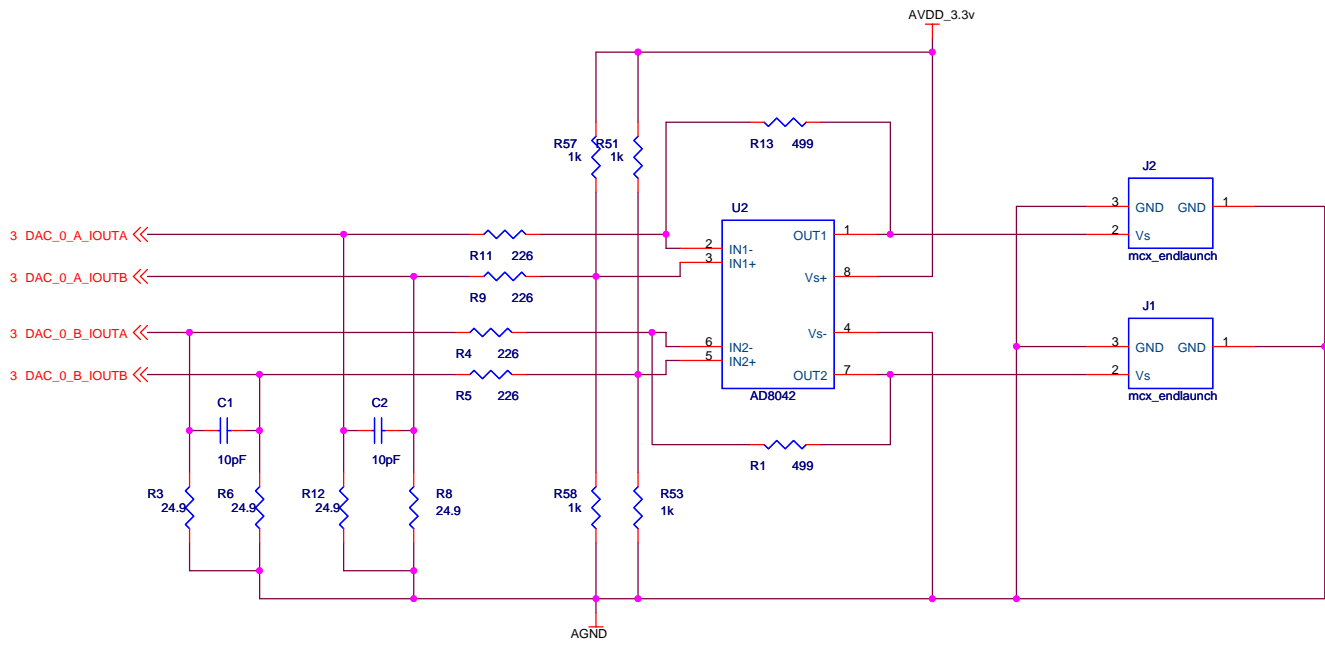
Pins [13,14] and [35,36] are the LSB data pins for the AD9767 which can be ignored for the pin compatible 12-bit AD9765. They're connected here for flexibility later.




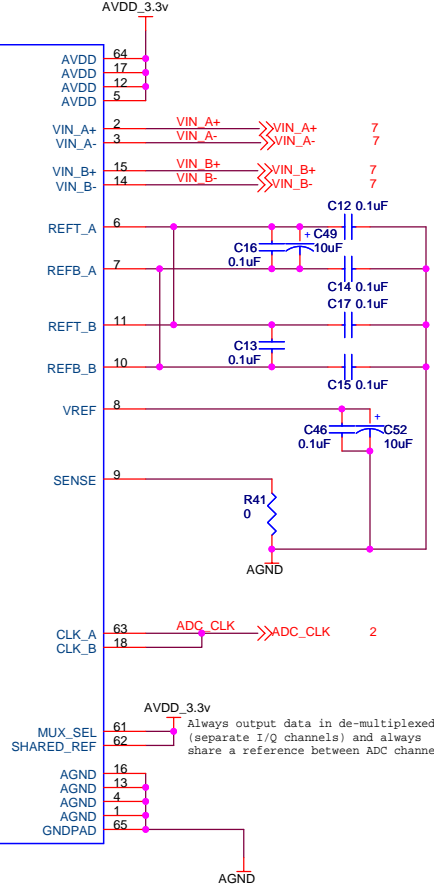
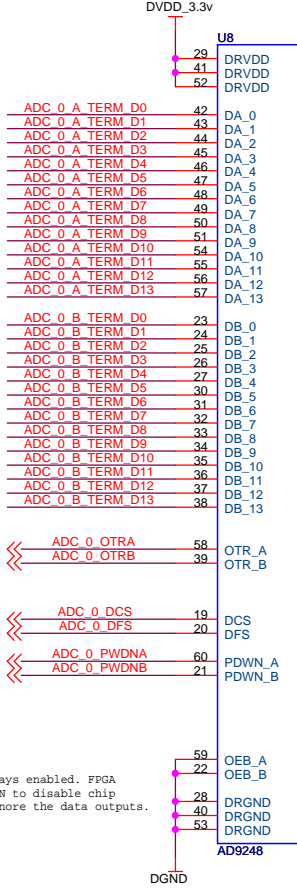
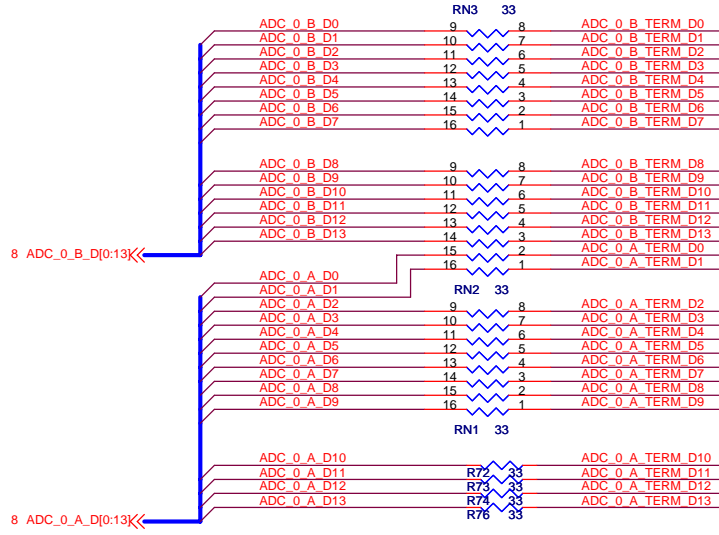
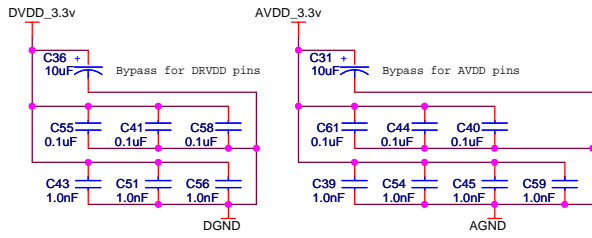


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|---|--------------|---|
| Center for Multimedia Communication Rice University | |  |
| Title ADC/DAC Daughtercard | | |
| Description Daughtercard for WARP Platform for Data Conversion | | Rev 1.1 |
| Date: Monday, September 18, 2006 | Sheet 5 of 9 | |



CHECK ME
 ADCs are configured to share a reference
 => REFX_A = REFX_B
 See pg. 15 of AD9238 datasheet

Outputs always enabled. FPGA
 can use PWDN to disable chip
 and just ignore the data outputs.

AVDD_3.3v
 Always output data in de-multiplexed mode
 (separate I/Q channels) and always
 share a reference between ADC channels

